

Advantech

AQD-SD5V8GN56-SC Datasheet

Rev. 1.0 2024-05-24



Description

AQD-SD5V8GN56-SC is DDR5-5600(CL46)-45-45 SDRAM memory module. The SPD is programmed to JEDEC standard latency 5600Mbps timing of 46-45-45 at 1.1V. The module is composed of 16Gb CMOS DDR5 SDRAMs in FBGA package and one 8Kbit SPD Hub in 8pin TDFN package on a 262pin glass–epoxy printed circuit board.

The module is a Dual In-line Memory Module and intended for mounting onto 262 pins edge connector sockets. Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features

- RoHS compliant products.
- JEDEC standard 1.1V(1.067V~1.166V) Power supply
- VDDQ= 1.1V(1.067V~1.166V)
- VPP = 1.8V(+0.108V / -0.054V)
- Data transfer rates: PC5-5600
- Programmable CAS Latency:
 22,26,28,30,32,36,40,42,46
- 16 bit pre-fetch
- Burst Length (BL) switch on-the-fly BL16 or BC8
- Bi-directional Differential Data-Strobe
- On Die Termination, Nominal, Park
- Serial presence detect hub (SPD Hub) with Integrated Temperature sensor
- Asynchronous reset
- PCB edge connector treated with 30u" Gold-Plating



Pin Descriptions

Pin Name	Description	Pin Name	Description
CA0_A - CA12_A CA0_B - CA12_B	SDRAM Command/Address bus	HSCL	Side Band bus clock
CS0_A_n - CS1_A_n CS0_B_n - CS1_B_n	SDRAM Chip Select	HSDA	Side Band bus data
DQ0_A - DQ31_A DQ0_B - DQ31_B	DIMM memory data bus	HSA	Side Band bus address
CB0_A - CB3_A CB0_B - CB3_B	DIMM ECC check bits	ALERT_n	SDRAM ALERT_n
DQS0_A_t - DQS4_A_t DQS0_B_t - DQS4_B_t	SDRAM data strobes (positive line of differential pair)	RESET_n	Set DRAMs to a Known State
DQS0_A_c - DQS4_A_c DQS0_B_c - DQS4_B_c	SDRAM data strobes (negative line of differential pair)	VIN_BULK	5 V power input supply
DM0_A_n - DM3_A_n DM0_B_n - DM3_B_n	SDRAM data masks	VSS	Power supply return (ground)
CK0_A_t, CK1_A_t CK0_B_t, CK1_B_t	SDRAM clocks (positive line of differential pair)	PWR_GOOD	Power good indicator
CK0_A_c, CK1_A_c CK0_B_c, CK1_B_c	SDRAM clocks (negative line of differential pair)	PWR_EN	PMIC Enable
		RFU	Reserved for future use

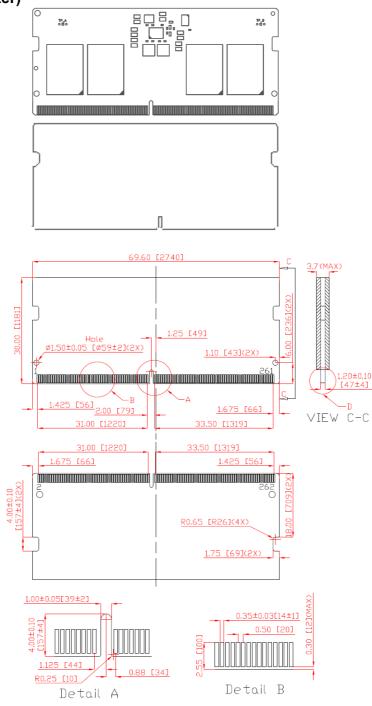
Notes:

DDR5 SO-DIMM has 2 channels (channel-A and channel-B) of signal bus.

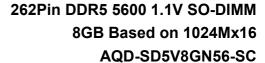
The signals with suffix: _A (e.g. DQ0_A) are for channel-A, and the signals with suffix: _B (e.g. DQ0_B) are for channel-B



Dimensions (Unit: millimeter)



Note:1. Tolerances on all dimensions +/-0.15mm unless otherwise specified.





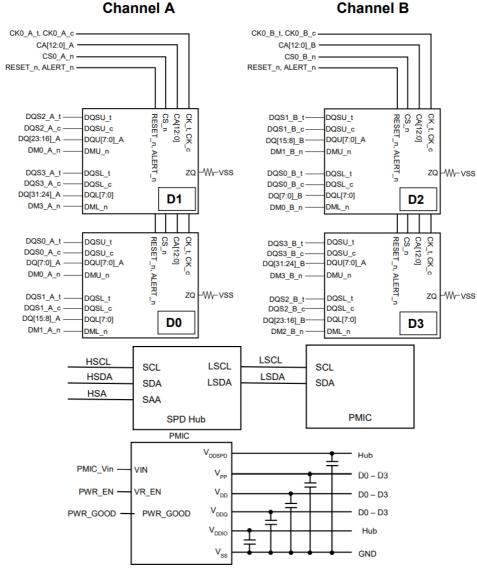
Pin Assignments

gnme	JIII S										
Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VIN_BULK	89	VSS	175	CB3_B	2	HSA	90	VSS	176	CB2_B
3	VIN_BULK	91	DQ30_A	177	VSS	4	HSCL	92	DQ31_A	178	VSS
5	RFU	93	VSS	179	DQ0_B	6	HSDA	94	VSS	180	DQ1_B
7	PWR_GOOD	95	CB0_A	181	VSS	8	PWR_EN	96	CB1_A	182	VSS
9	VSS	97	VSS	183	DQ2_B	10	VSS	98	VSS	184	DQ3_B
11	DQ0_A	99	CB2_A	185	VSS	12	DQ1_A	100	DQS4_A_c	186	VSS
13	VSS	101	VSS	187	DM0_B_n	14	VSS	102	DQS4_A_t	188	DQS0_B_c
15	DQ2_A	103	CB3_A	189	VSS	16	DQ3_A	104	VSS	190	DQS0_B_t
17	VSS	105	VSS	191	DQ4_B	18	VSS	106	CS0_A_n	192	VSS
19	DM0_A_n	107	CA0_A	193	VSS	20	DQS0_A_c	108	ALERT_n	194	DQ5_B
21	VSS	109	CA1_A	195	DQ6_B	22	DQS0_A_t	110	CS1_A_n	196	VSS
23	DQ4_A	111	VSS	197	VSS	24	VSS	112	VSS	198	DQ7_B
25	VSS	113	CA2_A	199	DQ8_B	26	DQ5_A	114	CA3_A	200	VSS
27	DQ6_A	115	CA4_A	201	VSS	28	VSS	116	CA5_A	202	DQ9_B
29	VSS	117	VSS	203	DQ10_B	30	DQ7_A	118	VSS	204	VSS
31	DQ8_A	119	CA6_A	205	VSS	32	VSS	120	CA7_A	206	DQ11_B
33	VSS	121	CA8_A	207	DQS1_B_c	34	DQ09_A	122	CA9_A	208	VSS
35	DQ10_A	123	VSS	209	DQS1_B_t	36	VSS	124	VSS	210	DM1_B_n
37	VSS	125	CA10_A	211	VSS	38	DQ11_A	126	CA11_A	212	VSS
39	DQS1_A_c	KEY		213	DQ12_B	40	VSS	KEY		214	DQ13_B
41	DQS1_A_t	127	CA12_A	215	VSS	42	DM1_A_n	128	RFU	216	VSS
43	VSS	129	VSS	217	DQ14_B	44	VSS	130	VSS	218	DQ15_B
45	DQ12_A	131	CK0_A_t	219	VSS	46	DQ13_A	132	CK1_A_t	220	VSS
47	VSS	133	CK0_A_c	221	DQ16_B	48	VSS	134	CK1_A_c	222	DQ17_B
49	DQ14_A	135	VSS	223	VSS	50	DQ15_A	136	VSS	224	VSS
51	VSS	137	CK0_B_t	225	DQ18_B	52	VSS	138	CK1_B_t	226	DQ19_B
53	DQ16_A	139	CK0_B_c	227	VSS	54	DQ17_A	140	CK1_B_c	228	VSS
55	VSS	141	VSS	229	DM2_B_n	56	VSS	142	VSS	230	DQS2_B_c
57	DQ18_A	143	RFU	231	VSS	58	DQ19_A	144	CA12_B	232	DQS2_B_t
59	VSS	145	CA11_B	233	DQ20_B	60	VSS	146	CA10_B	234	VSS
61	DM2_A_n	147	VSS	235	VSS	62	DQS2_A_c	148	VSS	236	DQ21_B
63	VSS	149	CA9_B	237	DQ22_B	64	DQS2_A_t	150	CA8_B	238	VSS
65	DQ20_A	151	CA7_B	239	VSS	66	VSS	152	CA6_B	240	DQ23_B
67	VSS	153	VSS	241	DQ24_B	68	DQ21_A	154	VSS	242	VSS
69	DQ22_A	155	CA5_B	243	VSS	70	VSS	156	CA4_B	244	DQ25_B
71	VSS	157	CA3_B	245	DQ26_B	72	DQ23_A	158	CA2_B	246	VSS
73	DQ24_A	159	VSS	247	VSS	74	VSS	160	VSS	248	DQ27_B
75	VSS	161	CS0_B_n	249	DQS3_B_c	76	DQ25_A	162	CA1_B	250	VSS
77	DQ26_A	163	RESET_n	251	DQS3_B_t	78	VSS	164	CA0_B	252	DM3_B_n
79	VSS	165	CS1_B_n	253	VSS	80	DQ27_A	166	VSS	254	VSS
81	DQS3_A_c	167	VSS	255	DQ28_B	82	VSS	168	CB0_B	256	DQ29_B
83	DQS3_A_t	169	DQS4_B_c	257	VSS	84	DM3_A_n	170	VSS	258	VSS
85	VSS	171	DQS4_B_t	259	DQ30_B	86	VSS	172	CB1_B	260	DQ31_B
87	DQ28_A	173	VSS	261	VSS	88	DQ29_A	174	VSS	262	VSS



Function Block Diagram

1Rank, x16 DDR5 SDRAMs



Note : ZQ resistors are $240\Omega \pm 1\%$.

This technical information is based on industry standard data and tests believed to be reliable. However, Advantech makes no warranties, either expressed or implied, as to its accuracy and assume no liability in connection with the use of this product. Advantech reserves the right to make changes in specifications at any time without prior notice.



Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Note
Operating Temperature	TOPER	0 to 85	°C	1,2

Note:

Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

Absolute Maximum DC Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on VDD relative to Vss	VDD	-0.3 ~ 1.4	V	1
Voltage on VDDQ pin relative to Vss	VDDQ	-0.3 ~ 1.4	V	1
Voltage on any pin relative to Vss	VIN, VOUT	-0.3 ~ 1.4	V	1
Storage temperature	Tstg	-55~+100	°C	1,2

Note:

- 1. Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- 2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

AC & DC Operating Conditions

Recommended DC operating conditions

Parameter	Cymphol	Voltage		Rating		Heis	Notes
Parameter	Symbol	Voltage	Min	Тур.	Max	Onne	Notes
Host Supply Voltage	VIN_BULK	12.0	4.25	5.0	5.5	V	
PMIC Output Supply Voltage	VDD	1.1	1.067	1.1	1.166	V	1,2,3
PMIC Output Supply Voltage	VDDQ	1.1	1.067	1.1	1.166	V	1,2,3
PMIC Output Supply Voltage	VPP	1.8	1.746	1.8	1,908	V	3
AC Input Logic High	VIH(AC)	TBD	-	-	-	mV	
AC Input Logic Low	VIL(AC)	TBD	-	-	-	mV	
DC Input Logic High	VIH(DC)	TBD	-	-	-	mV	
DC Input Logic Low	VIL(DC)	TBD	-	-	-	mV	

Note: (1) VDD must be within 66mv of VDDQ

- (2) AC parameters are measured with VDD and VDDQ tied together.
- (3) This includes all voltage noise from DC to 2 MHz at the DRAM package ball.



IDD Specification parameters Definition - 8GB

Symbol	Condition	8GB	Unit
IDD0	One bank ACTIVATE-PRECHARGE current	TBD	mA
IDD0F	Operating Four Bank Active-Precharge Current	TBD	mA
IDD2N	Precharge Standby Current	TBD	mA
IDD2P	Precharge Power-Down Current	TBD	mA
IDD3N	Active standby current	TBD	mA
IDD3P	Active Power-Down Current	TBD	mA
IDD4R	Burst Read Current	TBD	mA
IDD4W	Burst write current	TBD	mA
IDD5B	Burst Refresh Current (1x REF)	TBD	mA
IDD6N	Self refresh current: Normal temperature range (0–85°C)	TBD	mA
IDD7	Bank interleave read current	TBD	mA
IDD8	Maximum power-down current	TBD	mA



■ Timing Parameters & Specifications

		DDR5	-4800	DDR5	-5600	DDR5	-6400			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes	
			Clock	Timing						
Clock period average	tCK (AVG)	0.416	<0.454	0.357	<0.384	0.312	<0.333	ns	1	
			Command and	Address Timing	9					
Read to Read command delay for same bank group	tCCD_L	max(8nCK, 5ns)	-	max(8nCK, 5ns)	-	max(8nCK, 5ns)	-	nCK,ns	8	
Write to Write command delay for same bank groupp	tCCD_L_WR	max(32nCK, 20ns)	-	max(32nCK, 20ns)	-	max(32nCK, 20ns)	-	nCK,ns	8	
Write to Write command delay for same bank group, second write not RMW	tCCD_L_WR2	max(16nCK,	-	max(16nCK,	-	max(16nCK,	-	nCK,ns	8	
Read to Write command delay for same bank group	tCCD_L_RTW		CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE							
Write to Read command delay for same bank group	tCCD_L_WTR		CWL + WBL/2 + Max(16nCK,10ns)							
Read to Read command delay for different bank group	tCCD_S	8	8 - 8 - 8 -						8	
Write to Write command delay for different bank group	tCCD_S_WR	8	-	8	-	8	-	nCK	8	
Read to Write command delay for different bank group	tCCD_S_RTW	CL - CV	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE							
Write to Read command delay for different bank group	tCCD_S_WTR		C	WL + WBL/2 + N	lax(4nCK,2.5ns	;)		nCK,ns	4,6,8	
Write to Read with Auto Precharge command delay for same bank	tCCD_WTRA			CWL + WBL/2 ·	+ tWR - tRTP			nCK,ns	2,4,6,8	



	DDR5-4800 DDR5-5600 DDR5-6400								
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Activate to Activate command delay to same bank group for 1KB page size	tRRD_L(1K)	max(8nCK,	-	max(8nCK,	-	max(8nCK,	-	nCK,ns	8
Activate to Activate command delay to same bank group for 2KB page size	tRRD_L(2K)	max(8nCK, 5ns)	-	max(8nCK, 5ns)	-	max(8nCK, 5ns)	ı	nCK,ns	8
Activate to Activate command delay to different bank group for 1KB page size	tRRD_S(1K)	8	-	8	-	8	ı	nCK	8
Activate to Activate command delay to different bank group for 2KB page size	tRRD_S(2K)	8	-	8	-	8	-	nCK	8
Four activate window for 1KB page size	tFAW (1K)	Max(32nCK,	-	Max(32nCK, 11.428ns)	-	Max(32nCK, 10.000ns)	-	nCK,ns	
Four activate window for 2KB	tFAW (2K)	Max(40nCK, 16.666ns)	-	Max(40nCK, 14.285ns)	-	Max(40nCK, 12.500ns)	-	nCK,ns	
Read to Precharge command delay	tRTP	Max(12nCK, 7.5ns)	-	Max(12nCK, 7.5ns)	-	Max(12nCK, 7.5ns)	-	nCK,ns	8
Precharge to Precharge command delay	tPPD	2	-	2	-	2	-	nCK	7,8
Write recovery time	tWR	30	-	30	-	30	-	ns	8



Notes:

- 1. tCK(avg)min listed for reference only, refer to the Speed Bins and Operations section which lists all valid tCK(avg) values.
- 2. tCCD_WTRA(min) shall always be greater than or equal to CWL + WBL/2 + tWR(min) tRTP(min), and when using the appropriate rounding algorithms,
 - nCCD_WTRA(min) shall always be greater than or equal to CWL + WBL/2 + nWR(min) nRTP(min).
- 3. RBL: Read burst length associated with Read command
 - RBL = 32 (36 w/ RCRC on) for fixed BL32 and BL32 in BL32 OTF mode
 - RBL = 16 (18 w/ RCRC on) for fixed BL16 and BL16 in BL32 OTF mode
 - RBL = 16 (18 w/ RCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode
- 4. WBL: Write burst length associated with Write command
 - WBL = 32 (36 w/ WCRC on) for fixed BL32 and BL32 in BL32 OTF mode
 - WBL = 16 (18 w/ WCRC on) for fixed BL16 and BL16 in BL32 OTF mode
 - WBL = 16 (18 w/ WCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode
- 5. 5 The following is considered for tRTW equation
 - 1tCK needs to be added due to tDQS2CK
 - Read DQS offset timing can pull in the tRTW timing
 - 1tCK needs to be added when 1.5tCK postamble
- 6. CWL=CL-2
- 7. tPPD applies to any combination of precharge commands (PREab, PREsb, PREpb). tPPD also applies to any combination of precharge commands to a different die in a 3DS DDR5 SDRAM.
- 8. This parameter only specifies minimum values (there is no maximum value). The maximum value cells have been merged in the table to improve legibility.



SERIAL PRESENCE DETECT SPECIFICATION

Byte	Function Described	Function		HEX Value
0	Number of Bytes in SPD Device	SPD Total: 1024B	Bytes	30
1	SPD Revision for Base Configuration Parameters	Version 1.2		12
2	Key Byte / Host Bus Command Protocol Type	DDR5 SDRAM	М	12
3	Key Byte / Module Type	SO-DIMM		03
4	First SDRAM Density and Package	Monolithic SDRAM	16Gb	04
5	First SDRAM Addressing	Row: 16	Column: 10	00
6	First SDRAM I/O Width	x16		40
7	First SDRAM Bank Groups & Banks Per Bank Group	4 bank groups/4 banks po	er bank group	42
8	Second SDRAM Density and Package			00
9	Second SDRAM Addressing			00
10	Secondary SDRAM I/O Width			00
11	Second SDRAM Bank Groups & Banks Per Bank Group			00
12	SDRAM BL32 & Post Package Repair	One repair element per bank group Burst	t length 32 supported	90
13	SDRAM Duty Cycle Adjuster & Partial Array Self Refresh	Device supports DCA for 4-phas	se internal clock(s)	02
14	SDRAM Fault Handling	Writeback suppression or	ontrol in MR9	00
15	Reserved	must be coded as	0x00	00
16	SDRAM Nominal Voltage, VDD	Operable:1.1V	Endurant:1.1V	00
17	SDRAM Nominal Voltage, VDDQ		Endurant:1.1V	00
18	SDRAM Nominal Voltage, VPP		Endurant:1.8V	00
19	SDRAM Timing	Standard core timings pe	er JESD79-5	00
20	SDRAM Minimum Cycle Time (tCKAVGmin), Least Significant Byte			65
21	SDRAM Minimum Oycle Time (tCKAVGmin), Most Significant Byte	357 ps		01
22	SDRAM Maximum Cycle Time (tCKAVGmax), Least Significant Byte			F2
23	SDRAM Maximum Cycle Time (tCKAVGmax), Most Significant Byte	1010 ps		03
24	SDRAM CAS Latencies Supported: First Byte	CL22,26,28,30,	.32	7.4
25	SDRAM CAS Latencies Supported:Second Byte	CL,36,40,42,46		AD
26	SDRAM CAS Latencies Supported:Third Byte			00
27	SDRAM CAS Latencies Supported Fourth Byte			00
28	SDRAM CAS Latencies Supported Fifth Byte			00
29	Reserved	must be coded as	0x00	00
30	SDRAM Minimum CAS Latency Time (tAAmin), Least Significant Byte			80
31	SDRAM Minimum CAS Latency Time (tAAmin), Most Significant Byte	16000 ps		3E
32	SDRAM Minimum RAS to CAS Delay Time (IRCDmin), Least Significant Byte			80
33	SDRAM Minimum RAS to CAS Delay Time (IRCDmin), Most Significant Byte	16000 ps		3E
34	SDRAM Minimum Row Precharge Delay Time (IRPmin), Least Significant Byte			80
35	SDRAM Minimum Row Precharge Delay Time (IRPmin), Most Significant Byte	16000 ps		3E
36	SDRAM Minimum Active to Precharge Delay Time (IRASmin), Least Significant Nibble			00
37	SDRAM Minimum Active to Precharge Delay Time (tRASmin), Most Significant Byte	32000 ps		7D
38	SDRAM Minimum Active to Active/Refresh Delay Time (IRCmin), Least Significant Nibble			80
39	SDRAM Minimum Active to Active/Refresh Delay Time (RCmin), Most Significant Nibble	48000 ps		BB
40	SDRAM Minimum Write Recovery Time (fWRmin), Least Significant Nibble			30
41	SDRAM Minimum Write Recovery Time (tWRmin), Most Significant Nibble	30000 ps		75
42	SDRAM Minimum Refresh Recovery Delay Time (IRFC1min, IRFC1 sir min)Least Significant Byte			27
43	SDRAM Minimum Refresh Recovery Delay Time (IRFC1min, IRFC1 sir min),Most Significant Byte	295 ns		01
44	SDRAM Minimum Refresh Recovery Delay Time (IRFC2min, IRFC2 sir min)Least Significant Byte	400		Α0
45	SDRAM Minimum Refresh Recovery Delay Time (IRFC2min, IRFC2 sir min),Most Significant Byte	160 ns		00
46	SDRAM Minimum Refresh Recovery Delay Time (IRFCsbmin, IRFCsb sir min) Least Significant Byte			82
47	SDRAM Minimum Refresh Recovery Delay Time (IRFCsbmin, IRFCsb sir min) Most Significant Byte	130 ns		00
48	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(RRC1 dir min),Least Significant Byte			00
49	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(RRFC1 dir min),Most Significant Byte	monolithic SDR/	AMS	00
50	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(RRFC2 dir min),Least Significant Byte			00
51	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(RFC2_dlr min),Most Significant Byte	monolithic SDRA	AMs	00
52	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(RRFCsb dir min) Least Significant Byte			00
53	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(RRFCsb. dir min),Most Significant Byte	monolithic SDRA	AMs	00
54	SDRAM Refresh Management, First Byte, First SDRAM			00
55	SDRAM Refresh Management, Second Byte, First SDRAM			00
56	SDRAM Refresh Management, First Byte, Second SDRAM			00
57	SDRAM Refresh Management, Second Byte, Second SDRAM			00
58	SDRAM Adaptive Refresh Management, First SDRAM, First Byte, Level A			00
59	SDRAM Adaptive Refresh Management, First SDRAM, Second Byto,Level A			00
60	SDRAM Adaptive Refresh Management, Second SDRAM, First Byte, Level A			00



CORMA Adaptive Reflesh Management, First SDRAM, Second SPEAL Averil B SDRAM Adaptive Reflesh Management, First SDRAM, First BytuLevel B SDRAM Adaptive Reflesh Management, First SDRAM, Second SytuLevel B SDRAM Adaptive Reflesh Management, First SDRAM, Second SytuLevel B SDRAM Adaptive Reflesh Management, Second SDRAM, Second SytuLevel B SDRAM Adaptive Reflesh Management, First SDRAM, Second SytuLevel B SDRAM Adaptive Reflesh Management, First SDRAM, Second SytuLevel B SDRAM Adaptive Reflesh Management, First SDRAM, Second SytuLevel C SDRAM Adaptive Reflesh Management, First SDRAM, Second SytuLevel C SDRAM Adaptive Reflesh Management, First SDRAM, Second SytuLevel C SDRAM Adaptive Reflesh Management, First SDRAM, Second SytuLevel C SDRAM Management, Second SDRAM, Second SytuLevel C SDRAM Minimum Adaptive Adaptive Reflesh Management, Second SDRAM, Second SytuLevel C SDRAM Minimum Adaptive Adaptive Reflesh Management, Second SDRAM, Second SytuLevel C SDRAM Minimum Adaptive Adaptive Reflesh Management, Second SDRAM, Second SytuLevel C SDRAM Minimum Adaptive Adaptive Reflesh Management, Second SDRAM, Second Spram, Second SDRAM, Second SPRAM, Second Stram, Second SDRAM, Second SPRAM, Second Stram, Second SDRAM, Second SPRAM, Second SPR
SCRAM Adaptive Rafresh Management, First SCRAM, STRAM
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SDRAM Minimum Active to Active Command Delay Time, Same Bank Group, (SPRD Limin). Least Significant Byte 70 SDRAM Minimum Active to Active Command Delay Time, Same Bank Group, (SPRD Limin). Most Significant Byte 71 SDRAM Minimum Active to Active Command Delay Time, Same Bank Group, (SPRD Limin). Most Significant Byte 72 SDRAM Minimum Active to Active Command Delay Time, Same Bank Group, (SPRD Limin). Lover Clock Limit 8 InCK 73 SDRAM Minimum CAS in to CAS in Command Delay Time, Same Bank Group, (SCDD Limin). Lover Clock Limit 8 InCK 74 SDRAM Minimum CAS in to CAS in Command Delay Time, Same Bank Group, (SCDD Limin). Lover Clock Limit 8 InCK 75 SDRAM Minimum CAS in to CAS in Command Delay Time, Same Bank Group, (SCDD Limin). Lover Clock Limit 8 InCK 76 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group, (SCDD Limin). Lover Clock Limit 8 InCK 77 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group, (SCDD Limin). Lover Clock Limit 8 InCK 78 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group, (SCDD Limin). Lover Clock Limit 9 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group, (SCDD Limin). Lover Clock Limit 10 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group, (SCDD Limin). Lover Clock Limit 11 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group, (SCDD Limin). Lover Clock Limit 12 InCK 13 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group, (SCDD Limin). Lover Clock Limit 14 InCK 15 SDRAM Minimum Four Activate Window (SRAWrinin). Lover Significant Byte 16 InCK 17 SDRAM Minimum Four Activate Window (SRAWrinin). Lover Clock Limit 18 SDRAM Write to Read Command Delay for Same Bank Group, (SCDD Limin). Lover Clock Limit 19 SDRAM Write to Read Command Delay for Same Bank Group, (SCDD Limit). Lover Clock Limit 10 InCK 10 SDRAM Write to Read Command Delay for Different Bank Group, (SCDD Limit). Lover Clo
SDRAM Minimum Active to Active Command Delay Time, Same Bank Group, IRRD Limin, Least Significant Byte 70 SDRAM Minimum Active to Active Command Delay Time, Same Bank Group, IRRD Limin, Least Significant Byte 71 SDRAM Minimum Active to Active Command Delay Time, Same Bank Group, IRRD Limin, Least Significant Byte 72 SDRAM Minimum Active to Active Command Delay Time, Same Bank Group, IRRD Limin, Lower Clock Limit 73 SDRAM Minimum CAS in to CAS in Command Delay Time, Same Bank Group, IRRD Limin, Lower Clock Limit 74 SDRAM Minimum CAS in to CAS in Command Delay Time, Same Bank Group, IRCD Limin, Lower Clock Limit 75 SDRAM Minimum CAS in to CAS in Command Delay Time, Same Bank Group, IRCD Limin, Lower Clock Limit 76 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group, IRCD Limin, Lower Clock Limit 77 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group, IRCD Limin, Lower Clock Limit 78 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group, IRCD Limin, Lower Clock Limit 79 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group, IRCD Limin, Lower Clock Limit 79 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group, IRCD Limin, Lower Clock Limit 80 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group, IRCD Limin, Lower Clock Limit 81 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group, IRCD Limin, Lower Clock Limit 82 SDRAM Minimum Four Activate Window (FAWrinin) Loads Significant Byte 83 SDRAM Minimum Four Activate Window (FAWrinin) Loads Significant Byte 84 SDRAM Minimum Four Activate Window (FAWrinin) Loads Significant Byte 85 SDRAM Write to Read Command Delay for Same Bank Group, IRCD Limit, Lower Clock Limit 86 SDRAM Write to Read Command Delay for Same Bank Group, IRCD Limit, Lower Clock Limit 86 SDRAM Write to Read Command Delay for Same Bank Group, IRCD Limit, Lower Clock Limit 87 SDRAM Write to Read Command Delay
TO SDRAM Minimum Active to Active Command Delay Time, Same Bank Group, (RRD Limin). Least Significant Byte 3 SDRAM Minimum Active to Active Command Delay Time, Same Bank Group, (RRD Limin). Least Significant Byte 3 SDRAM Minimum CAS in to CAS in Command Delay Time, Same Bank Group, (RDD Limin). Least Significant Byte 5 SDRAM Minimum CAS in to CAS in Command Delay Time, Same Bank Group, (RDD Limin). Least Significant Byte 5 SDRAM Minimum CAS in to CAS in Command Delay Time, Same Bank Group, (RDD Limin). Least Significant Byte 5 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group, (RDD Limin). Least Significant Byte 5 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group, (RDD Limin). Least Significant Byte 5 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group, (RDD Limin). Least Significant Byte 5 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group, (RDD Limin). Least Significant Byte 5 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group, (RDD Limin). Least Significant Byte 5 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group, (RDD Limin). Least Significant Byte 8 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group, (RDD Limin). Least Significant Byte 8 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group, (RDD Limin). Least Significant Byte 8 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group, (RDD Limin). Least Significant Byte 8 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group, (RDD Limin). Least Significant Byte 8 SDRAM Write to Rada Command Delay Minimum Bank Group, (RDD Limit). Least Significant Byte 9 SDRAM Write to Rada Command Delay for Same Bank Group, (RDD Limit). Least Significant Byte 9 SDRAM Write to Rada Command Delay for Same Bank Group, (RDD Limit). Least Significant Byte 9 SDRAM Write to Rada Command Delay for
T1 SDRAM Minimum Active to Active Command Delay Time, Same Bank Group,ISRD Lmin]Most Significant Byte 72 SDRAM Minimum Active to Active Command Delay Time, Same Bank Group,ISRD Lmin]Lower Clock Limit 73 SDRAM Minimum CAS in to CAS in Command Delay Time, Same Bank Group,ISCDD Lmin]Lower Clock Limit 74 SDRAM Minimum CAS in to CAS in Command Delay Time, Same Bank Group,ISCDD Lmin]Lower Clock Limit 75 SDRAM Minimum CAS in to CAS in Command Delay Time, Same Bank Group,ISCDD Lmin]Lower Clock Limit 76 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group,ISCDD L WRItin]Lower Clock Limit 77 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group,ISCDD L WRItin]Lower Clock Limit 78 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group,ISCDD L WRItin]Lower Clock Limit 79 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group,ISCDD L WRItin]Lower Clock Limit 80 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group,ISCDD L WRItin]Lower Clock Limit 81 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group,ISCDD L WRItin]Lower Clock Limit 82 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group,ISCDD L WRItin]Lower Clock Limit 83 SDRAM Minimum Four Activate Wrindow SRAWmin]Lower Significant Byte 84 SDRAM Minimum Four Activate Wrindow SRAWmin]Lower Clock Limit 85 SDRAM Minimum Four Activate Wrindow SRAWmin]Lower Clock Limit 86 SDRAM Write to Read Command Delay for Same Bank Group,ISCDD L WRITH, Lower Significant Byte 87 SDRAM Write to Read Command Delay for Same Bank Group,ISCDD L WRITH, Lower Significant Byte 88 SDRAM Write to Read Command Delay for Same Bank Group,ISCDD S WRITH, Lower Significant Byte 90 SDRAM Write to Read Command Delay SRTP, SRTP SrI, Lower Clock Limit 91 SDRAM Read to Prechapse Command Delay SRTP, SRTP SrI, Lower Clock Limit 92 SDRAM Read to Prechapse Command Delay SRTP, SRTP SrI, Lower Clock Limit 93 SDRAM Read to
T1 SDRAM Minimum Active to Active Command Delay Time, Same Bank Group, PRD Limin Julover Clock Limit SDRAM Minimum CAS n to CAS n Command Delay Time, Same Bank Group, PRD Limin Julover Clock Limit SDRAM Minimum CAS n to CAS n Command Delay Time, Same Bank Group, PCCD Limin Julover Clock Limit SDRAM Minimum CAS n to CAS n Command Delay Time, Same Bank Group, PCCD Limin Julover Clock Limit SDRAM Minimum CAS n to CAS n Command Delay Time, Same Bank Group, PCCD Limin Julover Clock Limit SDRAM Minimum Write CAS n to Write CAS n Command Delay Time, Same Bank Group (CCD L WRitin Julover Clock Limit SDRAM Minimum Write CAS n to Write CAS n Command Delay Time, Same Bank Group (CCD L WRitin Julover Clock Limit SDRAM Minimum Write CAS n to Write CAS n Command Delay Time, Same Bank Group (CCD L WRitin Julover Clock Limit SDRAM Minimum Write CAS n to Write CAS n Command Delay Time, Same Bank Group (CCD L WRItin Julover Clock Limit SDRAM Minimum Write CAS n to Write CAS n Command Delay Time, Same Bank Group (CCD L WRItin Julover Clock Limit SDRAM Minimum Write CAS n to Write CAS n Command Delay Time, Same Bank Group (CCD L WRItin Julover Clock Limit SDRAM Minimum Write CAS n to Write CAS n Command Delay Time, Same Bank Group (CCD L WRItin Julover Clock Limit SDRAM Minimum Write CAS n to Write CAS n Command Delay Time, Same Bank Group (CCD L WRItin Julover Clock Limit SDRAM Write CAS n to Write CAS n Command Delay Time, Same Bank Group (CCD L WRITIN Julover Clock Limit SDRAM Write CAS n to Write CAS n Command Delay Time, Same Bank Group (CCD L WRITIN Julover Clock Limit SDRAM Write CAS n to Write CAS n Command Delay Time, Same Bank Group (CCD L WRITIN Julover Clock Limit SDRAM Write CAS n to Write CAS n Command Delay Time, Same Bank Group (CCD L WRITIN Julover Clock Limit SDRAM Write CAS n to Write CAS n Command Delay Time, Same Bank Group (CCD L WRITIN Julover Clock Limit SDRAM Write to Read Command Delay for Different Bank Group (CCD S WRIT, Least Significant Byte SDRAM Write to Read Command Delay for Dif
SDRAM Minimum CAS in to CAS in Command Delay Time, Same Bank Group,(ICCD Limin)Least Significant Byte 5000 ps
73 SCRAM Minimum CAS in to CAS in Command Delay Time, Same Bank Group, (CCC) Limin) Least Significant Byte 74 SCRAM Minimum CAS in to CAS in Command Delay Time, Same Bank Group, (CCC) Limin) Lower Clock Limit 75 SCRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group, (CCC) Limin) Lower Clock Limit 8 nCK 76 SCRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group, (CCC) Limin) Lower Clock Limit 8 nCK 77 SCRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group, (CCC) Limin) Lower Clock Limit 9 SCRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group, (CCC) Limin) Lower Clock Limit 9 SCRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group, (CCC) Limin) Lower Clock Limit 9 SCRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group, (CCC) Limin) Lower Clock Limit 1000 pc 8 SCRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group, (CCC) Limin) Lower Clock Limit 11 SCRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group, (CCC) Limin) Lower Clock Limit 12 SCRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group, (CCC) Limin) Lower Clock Limit 14 SCRAM Minimum Four Activate Write CAS in Command Delay Time, Same Bank Group, (CCC) Limin) Lower Clock Limit 15 SCRAM Write to Read Command Delay Minimum Sclignificant Byte 16 SCRAM Write to Read Command Delay for Same Bank Group, (CCC) Limit 17 SCRAM Write to Read Command Delay for Same Bank Group, (CCC) Limit 18 SCRAM Write to Read Command Delay for Same Bank Group, (CCC) Limit 19 SCRAM Write to Read Command Delay for Same Bank Group, (CCC) Simit, Lower Clock Limit 19 SCRAM Write to Read Command Delay for Different Bank Group, (CCC) Simit, Lower Clock Limit 19 SCRAM Read to Precharge Command Delay (RTP, RTP sir), Least Significant Byte 10 SCRAM Read to Precharge Command Delay (RTP, RTP sir), Lower Clock Limit 11 SCRAM Read to Precharge Command Delay (RTP, RTP sir), Lower Clock Li
SDRAM Minimum CAS in to CAS in Command Delay Time, Same Bank Group,(ICCD Limin), Most Significant Byte 5 SDRAM Minimum With CAS in to Write CAS in Command Delay Time, Same Bank Group,(ICCD Limin), With CAS in Command Delay Time, Same Bank Group, ICCD Limin), With CAS in Command Delay Time, Same Bank Group, ICCD Limin), With CAS in Command Delay Time, Same Bank Group, ICCD Limin), With CAS in Command Delay Time, Same Bank Group, ICCD Limin, With CAS in Command Delay Time, Same Bank Group, ICCD Limin, Case Command Delay Time, Same Bank Group, ICCD Limin, Case Command Case
SDRAM Minimum CAS in to CAS in Command Delay Time, Same Bank Group,(CCD L Min),Lower Clock Limit 75 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (CCD L WRmin),Least Significant Byte 20000 ps 78 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (CCD L WRmin),Lower Clock Limit 79 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (CCD L WRmin),Lower Clock Limit 80 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (CCD L WRZmin),Loast Significant Byte 81 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (CCD L WRZmin),Loast Significant Byte 82 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (CCD L WRZmin),Loast Significant Byte 83 SDRAM Minimum Four Activate Wrindow (FAWmin),Loast Significant Byte 84 SDRAM Minimum Four Activate Wrindow (FAWmin),Loast Significant Byte 85 SDRAM Write to Read Command Delay for Same Bank Group (CCD L WTR), Most Significant Byte 86 SDRAM Write to Read Command Delay for Same Bank Group (CCD L WTR), Most Significant Byte 87 SDRAM Write to Read Command Delay for Same Bank Group (CCD L WTR), Most Significant Byte 88 SDRAM Write to Read Command Delay for Same Bank Group (CCD S WTR), Loast Significant Byte 89 SDRAM Write to Read Command Delay for Different Bank Group (CCD S WTR), Loast Significant Byte 90 SDRAM Write to Read Command Delay for Different Bank Group (CCD S WTR), Loast Significant Byte 91 SDRAM Read to Precharge Command Delay for Different Bank Group (CCD S WTR), Loast Significant Byte 92 SDRAM Read to Precharge Command Delay for Different Bank Group (CCD S WTR), Loast Significant Byte 93 SDRAM Read to Precharge Command Delay for Different Bank in Same Bank Group (CCD M), Loast Significant Byte 94 SDRAM Read to Precharge Command Delay for Different Bank in Same Bank Group (CCD M), Loast Significant Byte 95 SDRAM Read to Precharge Command Delay for Different Bank in Same Bank Group (
TO SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (tCCD L. WRmin) Least Significant Byte 2000 ps 3 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (tCCD L. WRmin) Library Clock Limit 32 in CK 79 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (tCCD L. WRZmin) Library Clock Limit 30 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (tCCD L. WRZmin) Library Clock Limit 31 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (tCCD L. WRZmin) Library Significant Byte 32 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (tCCD L. WRZmin) Lover Clock Limit 33 SDRAM Minimum Four Activate Window (tFAWmin) Library Time, Same Bank Group (tCCD L. WRZmin) Lover Clock Limit 44 SDRAM Minimum Four Activate Window (tFAWmin) Library Clock Limit 45 SDRAM Write to Read Command Delay for Same Bank Group (tCCD L. WTR) Library Significant Byte 56 SDRAM Write to Read Command Delay for Same Bank Group (tCCD L. WTR) Library Clock Limit 57 SDRAM Write to Read Command Delay for Same Bank Group (tCCD L. WTR) Library Clock Limit 58 SDRAM Write to Read Command Delay for Same Bank Group (tCCD L. WTR) Library Clock Limit 59 SDRAM Write to Read Command Delay for Different Bank Group (tCCD S. WTR) Least Significant Byte 50 SDRAM Write to Read Command Delay for Different Bank Group (tCCD S. WTR) Least Significant Byte 50 SDRAM Write to Read Command Delay for Different Bank Group (tCCD S. WTR) Least Significant Byte 50 SDRAM Write to Read Command Delay for Different Bank Group (tCCD S. WTR) Least Significant Byte 51 SDRAM Read to Precharge Command Delay (tRTP, tRTP sir), Least Significant Byte 52 SDRAM Read to Precharge Command Delay (tRTP, tRTP sir), Least Significant Byte 53 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (tCCD M) Library Clock Limit 54 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (tCC
77 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (tCCD L. WRimin),Most Significant Byte 2000 ps SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (tCCD L. WRimin),Lower Clock Limit 32 inCK SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (tCCD L. WRimin),Lower Clock Limit 80 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (tCCD L. WRimin),Lower Clock Limit 81 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (tCCD L. WRite),Lower Clock Limit 82 SDRAM Minimum Four Activate Window (FAWmin),Loast Significant Byte 83 SDRAM Minimum Four Activate Window (FAWmin),Most Significant Byte 84 SDRAM Minimum Four Activate Window (FAWmin),Lower Clock Limit 85 SDRAM Write to Read Command Delay tor Same Bank Group (tCCD L. WTR), Most Significant Byte 86 SDRAM Write to Read Command Delay tor Same Bank Group (tCCD L. WTR), Most Significant Byte 87 SDRAM Write to Read Command Delay tor Same Bank Group (tCCD L. WTR), Most Significant Byte 88 SDRAM Write to Read Command Delay tor Same Bank Group (tCCD L. WTR), Most Significant Byte 89 SDRAM Write to Read Command Delay tor Same Bank Group (tCCD S. WTR), Most Significant Byte 89 SDRAM Write to Read Command Delay tor Different Bank Group (tCCD S. WTR), Lower Clock Limit 90 SDRAM Write to Read Command Delay tor Different Bank Group (tCCD S. WTR), Lower Clock Limit 91 SDRAM Read to Read Command Delay tor Different Bank Group (tCCD S. WTR), Lower Clock Limit 92 SDRAM Read to Read Command Delay tor Different Bank Group (tCCD S. WTR), Lower Clock Limit 93 SDRAM Read to Read Command Delay tor Different Bank in Same Bank Group (tCCD M.), Most Significant Byte 94 SDRAM Read to Read Command Delay tor Different Bank in Same Bank Group (tCCD M.), Most Significant Byte 95 SDRAM Read to Read Command Delay tor Different Bank in Same Bank Group (tCCD M.), Most Significant Byte 96 SDRAM Write to Write Command Delay tor Different B
78 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (CCCD L. WRitin), Lower Clock Limit 79 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (CCCD L. WRZmin), Least Significant Byte 80 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (CCCD L. WRZmin), Least Significant Byte 81 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (CCCD L. WRZmin), Least Significant Byte 82 SDRAM Minimum Four Activate Window (FAWmin), Least Significant Byte 83 SDRAM Minimum Four Activate Window (FAWmin), Lower Clock Limit 84 SDRAM Minimum Four Activate Window (FAWmin), Lower Clock Limit 85 SDRAM Write to Read Command Delay for Same Bank Group (CCCD L. WRR), Least Significant Byte 86 SDRAM Write to Read Command Delay for Same Bank Group (CCCD L. WRR), Lower Clock Limit 87 SDRAM Write to Read Command Delay for Same Bank Group (CCCD L. WRR), Lower Clock Limit 88 SDRAM Write to Read Command Delay for Same Bank Group (CCCD L. WRR), Lower Clock Limit 89 SDRAM Write to Read Command Delay for Same Bank Group (CCCD S. WRR), Loast Significant Byte 90 SDRAM Write to Read Command Delay for Different Bank Group (CCCD S. WRR), Loast Significant Byte 90 SDRAM Write to Read Command Delay for Different Bank Group (CCCD S. WRR), Loast Significant Byte 91 SDRAM Write to Read Command Delay for Different Bank Group (CCCD S. WRR), Loast Significant Byte 92 SDRAM Write to Read Command Delay for Different Bank Group (CCCD S. WRR), Lower Clock Limit 93 SDRAM Read to Precharge Command Delay (RTP, RTP SIr), Loast Significant Byte 94 SDRAM Read to Precharge Command Delay (RTP, RTP SIr), Lower Clock Limit 95 SDRAM Read to Precharge Command Delay (RTP, RTP SIr), Lower Clock Limit 96 SDRAM Read to Precharge Command Delay (RTP, RTP SIr), Lower Clock Limit 97 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (CCCD M), Lower Clock Limit 98 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (CCCD M), Lower Cloc
SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (ICCD L. WRZmin),Lower Clock Limit 79 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (ICCD L. WRZmin),Loast Significant Byte 80 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (ICCD L. WRZmin),Loast Significant Byte 81 SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (ICCD L. WRZmin),Lower Clock Limit 82 SDRAM Minimum Four Activate Window (IFAWmin),Loast Significant Byte 83 SDRAM Minimum Four Activate Window (IFAWmin),Loast Significant Byte 84 SDRAM Minimum Four Activate Window (IFAWmin),Lower Clock Limit 85 SDRAM Minimum Four Activate Window (IFAWmin),Lower Clock Limit 86 SDRAM Write to Read Command Delay for Same Bank Group (ICCD L. WTR),Loast Significant Byte 86 SDRAM Write to Read Command Delay for Same Bank Group (ICCD L. WTR),Lower Clock Limit 87 SDRAM Write to Read Command Delay for Same Bank Group (ICCD L. WTR),Lower Clock Limit 88 SDRAM Write to Read Command Delay for Different Bank Group (ICCD S. WTR), Lower Clock Limit 89 SDRAM Write to Read Command Delay for Different Bank Group (ICCD S. WTR), Lower Clock Limit 90 SDRAM Write to Read Command Delay for Different Bank Group (ICCD S. WTR), Lower Clock Limit 91 SDRAM Read to Precharge Command Delay (IRTP, IRTP Sir), Loast Significant Byte 92 SDRAM Read to Precharge Command Delay (IRTP, IRTP Sir), Lower Clock Limit 93 SDRAM Read to Read Command Delay (IRTP, IRTP Sir), Lower Clock Limit 94 SDRAM Read to Read Command Delay (IRTP, IRTP Sir), Lower Clock Limit 95 SDRAM Read to Read Command Delay (IRTP, IRTP Sir), Lower Clock Limit 96 SDRAM Read to Read Command Delay (IRTP, IRTP Sir), Lower Clock Limit 97 SDRAM Read to Read Command Delay (IRTP) Sir) Same Bank Group (ICCD M.), Lower Clock Limit 98 SDRAM Read to Read Command Delay (IRTP) Sir) Same Bank Group (ICCD M.), Lower Clock Limit 99 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (ICCD M.)
SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (tCCD L WRZmin),Least Significant Byte SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (tCCD L WRZmin),Most Significant Byte SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (tCCD L WRZmin),Lower Clock Limit SDRAM Minimum Four Activate Window (FAWmin),Most Significant Byte SDRAM Write to Read Command Delay for Same Bank Group (tCCD L WTR),Least Significant Byte SDRAM Write to Read Command Delay for Same Bank Group (tCCD L WTR), Most Significant Byte SDRAM Write to Read Command Delay for Same Bank Group (tCCD L WTR), Least Significant Byte SDRAM Write to Read Command Delay for Different Bank Group (tCCD S WTR), Least Significant Byte SDRAM Write to Read Command Delay for Different Bank Group (tCCD S WTR), Least Significant Byte SDRAM Write to Read Command Delay for Different Bank Group (tCCD S WTR), Least Significant Byte SDRAM Write to Read Command Delay for Different Bank Group (tCCD S WTR), Least Significant Byte SDRAM Write to Read Command Delay for Different Bank Group (tCCD S WTR), Lower Clock Limit 4 nCK SDRAM Read to Precharge Command Delay (tRTP, tRTP sir), Least Significant Byte SDRAM Read to Precharge Command Delay (tRTP, tRTP sir), Lower Clock Limit SDRAM Read to Precharge Command Delay (tRTP, tRTP sir), Lower Clock Limit SDRAM Read to Precharge Command Delay (trTP, tRTP sir), Lower Clock Limit SDRAM Read to Precharge Command Delay (trTP, trTP sir), Most Significant Byte SDRAM Read to Precharge Command Delay (trTP, trTP sir), Most Significant Byte SDRAM Read to Read Command Delay to Different Bank in Same Bank Group (tCCD M), Most Significant Byte SDRAM Write to Write Command Delay to Different Bank in Same Bank Group (tCCD M), Most Significant B
SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (tCCD L. WRZmin), Most Significant Byte 81 SDRAM Minimum Write CAS in command Delay Time, Same Bank Group (tCCD L. WRZmin), Lower Clock Limit 82 SDRAM Minimum Four Activate Window (tFAWmin), Lloest Significant Byte 83 SDRAM Minimum Four Activate Window (tFAWmin), Lloest Significant Byte 84 SDRAM Minimum Four Activate Window (tFAWmin), Lloest Significant Byte 85 SDRAM Write to Read Command Delay for Same Bank Group (tCCD L. WTR), Lloest Significant Byte 86 SDRAM Write to Read Command Delay for Same Bank Group (tCCD L. WTR), Lloest Significant Byte 87 SDRAM Write to Read Command Delay for Same Bank Group (tCCD L. WTR), Lloest Significant Byte 88 SDRAM Write to Read Command Delay for Different Bank Group (tCCD S. WTR), Lloest Significant Byte 89 SDRAM Write to Read Command Delay for Different Bank Group (tCCD S. WTR), Lloest Significant Byte 90 SDRAM Write to Read Command Delay for Different Bank Group (tCCD S. WTR), Lloest Significant Byte 91 SDRAM Read to Read Command Delay for Different Bank Group (tCCD S. WTR), Lloest Clock Limit 92 SDRAM Read to Precharge Command Delay (tRTP, tRTP sir), Lloest Significant Byte 93 SDRAM Read to Precharge Command Delay (tRTP, tRTP sir), Lloest Significant Byte 94 SDRAM Read to Read Command Delay (tRTP, tRTP sir), Lower Clock Limit 95 SDRAM Read to Read Command Delay (trtp, tRTP sir), Lower Clock Limit 96 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (tCCD M), Lloest Significant Byte 97 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (tCCD M), Lloest Significant Byte 98 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M), Lloest Significant Byte 89 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M), Lloest Significant Byte 80 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M), WR), Lloest Significant Byte 80 SDRAM Write to Write Command Delay
SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (CCD L. WRZmin), Most Significant Byte SDRAM Minimum Four Activate Window (FAWmin), Loast Significant Byte SDRAM Minimum Four Activate Window (FAWmin), Most Significant Byte SDRAM Minimum Four Activate Window (FAWmin), Loast Significant Byte SDRAM Minimum Four Activate Window (FAWmin), Loast Significant Byte SDRAM Write to Read Command Delay for Same Bank Group (CCD L. WTR), Loast Significant Byte SDRAM Write to Read Command Delay for Same Bank Group (CCD L. WTR), Loast Significant Byte SDRAM Write to Read Command Delay for Same Bank Group (CCD S. WTR), Loast Significant Byte SDRAM Write to Read Command Delay for Different Bank Group (CCD S. WTR), Loast Significant Byte SDRAM Write to Read Command Delay for Different Bank Group (CCD S. WTR), Loast Significant Byte SDRAM Write to Read Command Delay for Different Bank Group (CCD S. WTR), Loast Significant Byte SDRAM Write to Read Command Delay for Different Bank Group (CCD S. WTR), Loast Significant Byte SDRAM Read to Precharge Command Delay (RTP, RTP sir), Loast Significant Byte SDRAM Read to Precharge Command Delay (RTP, RTP sir), Loast Significant Byte SDRAM Read to Precharge Command Delay (RTP, RTP sir), Loast Significant Byte SDRAM Read to Read Command Delay (RTP, RTP sir), Loast Significant Byte SDRAM Read to Read Command Delay (RTP, RTP sir), Loast Significant Byte SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (CCD M), Most Significant Byte SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (CCD M), Most Significant Byte SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (CCD M), Most Significant Byte SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (CCD M), Most Significant Byte SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (CCD M), WR), Least Significant Byte SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (CCD M), W
SDRAM Minimum Four Activate Window (#AWmin),Least Significant Byte 83 SDRAM Minimum Four Activate Window (#AWmin),Most Significant Byte 84 SDRAM Minimum Four Activate Window (#AWmin),Lower Clock Limit 85 SDRAM Write to Read Command Delay for Same Bank Group (tCCD L WTR), Most Significant Byte 86 SDRAM Write to Read Command Delay for Same Bank Group (tCCD L WTR), Most Significant Byte 87 SDRAM Write to Read Command Delay for Same Bank Group (tCCD L WTR), Most Significant Byte 88 SDRAM Write to Read Command Delay for Different Bank Group (tCCD S WTR), Least Significant Byte 89 SDRAM Write to Read Command Delay for Different Bank Group (tCCD S WTR), Most Significant Byte 90 SDRAM Write to Read Command Delay for Different Bank Group (tCCD S WTR), Most Significant Byte 91 SDRAM Read to Precharge Command Delay for Different Bank Group (tCCD S WTR), Lower Clock Limit 92 SDRAM Read to Precharge Command Delay (tRTP, tRTP sir), Least Significant Byte 93 SDRAM Read to Precharge Command Delay (tRTP, tRTP sir), Most Significant Byte 94 SDRAM Read to Read Command Delay (tRTP, tRTP sir), Lower Clock Limit 95 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (tCCD M), Least Significant Byte 96 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (tCCD M), Most Significant Byte 97 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (tCCD M), Most Significant Byte 98 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M), Most Significant Byte 99 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M), Most Significant Byte 89 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M), WR), Most Significant Byte 80 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M) WR), Most Significant Byte
SDRAM Minimum Four Activate Window (#AWmin),Least Significant Byte 83 SDRAM Minimum Four Activate Window (#AWmin),Most Significant Byte 84 SDRAM Minimum Four Activate Window (#AWmin),Lower Clock Limit 85 SDRAM Write to Read Command Delay for Same Bank Group (tCCD L WTR), Most Significant Byte 86 SDRAM Write to Read Command Delay for Same Bank Group (tCCD L WTR), Most Significant Byte 87 SDRAM Write to Read Command Delay for Same Bank Group (tCCD L WTR), Most Significant Byte 88 SDRAM Write to Read Command Delay for Different Bank Group (tCCD S WTR), Least Significant Byte 89 SDRAM Write to Read Command Delay for Different Bank Group (tCCD S WTR), Most Significant Byte 90 SDRAM Write to Read Command Delay for Different Bank Group (tCCD S WTR), Most Significant Byte 91 SDRAM Read to Precharge Command Delay for Different Bank Group (tCCD S WTR), Lower Clock Limit 92 SDRAM Read to Precharge Command Delay (tRTP, tRTP sir), Least Significant Byte 93 SDRAM Read to Precharge Command Delay (tRTP, tRTP sir), Most Significant Byte 94 SDRAM Read to Read Command Delay (tRTP, tRTP sir), Lower Clock Limit 95 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (tCCD M), Least Significant Byte 96 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (tCCD M), Most Significant Byte 97 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (tCCD M), Most Significant Byte 98 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M), Most Significant Byte 99 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M), Most Significant Byte 89 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M), WR), Most Significant Byte 80 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M) WR), Most Significant Byte
SDRAM Minimum Four Activate Window (#AWmin],Most Significant Byte 84 SDRAM Minimum Four Activate Window (#AWmin],Lower Clock Limit 85 SDRAM Write to Read Command Delay for Same Bank Group (tCCD L WTR), Loast Significant Byte 86 SDRAM Write to Read Command Delay for Same Bank Group (tCCD L WTR), Most Significant Byte 87 SDRAM Write to Read Command Delay for Different Bank Group (tCCD S WTR), Loast Significant Byte 88 SDRAM Write to Read Command Delay for Different Bank Group (tCCD S WTR), Loast Significant Byte 89 SDRAM Write to Read Command Delay for Different Bank Group (tCCD S WTR), Loast Significant Byte 90 SDRAM Write to Read Command Delay for Different Bank Group (tCCD S WTR), Loast Significant Byte 91 SDRAM Read to Precharge Command Delay (tRTP, RTP sir), Least Significant Byte 92 SDRAM Read to Precharge Command Delay (tRTP, RTP sir), Most Significant Byte 93 SDRAM Read to Precharge Command Delay (tRTP, RTP sir), Loast Significant Byte 94 SDRAM Read to Read Command Delay (tRTP, RTP sir), Loast Significant Byte 95 SDRAM Read to Read Command Delay (trtp, RTP sir), Lower Clock Limit 96 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (tCCD M), Most Significant Byte 97 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (tCCD M), Most Significant Byte 98 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M), Most Significant Byte 99 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M), WR), Least Significant Byte 99 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M), WR), Least Significant Byte 90 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M), WR), Least Significant Byte 90 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M), WR), Least Significant Byte 90 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M), WR), Least Significant Byte
SDRAM Minimum Four Activate Window (E-AWmin), Lower Clock Limit 84 SDRAM Minimum Four Activate Window (E-AWmin), Lower Clock Limit 85 SDRAM Write to Read Command Delay for Same Bank Group (tCCD L WTR), Most Significant Byte 86 SDRAM Write to Read Command Delay for Same Bank Group (tCCD L WTR), Most Significant Byte 87 SDRAM Write to Read Command Delay for Same Bank Group (tCCD L WTR), Most Significant Byte 88 SDRAM Write to Read Command Delay for Different Bank Group (tCCD S WTR), Least Significant Byte 89 SDRAM Write to Read Command Delay for Different Bank Group (tCCD S WTR), Most Significant Byte 90 SDRAM Write to Read Command Delay for Different Bank Group, (tCCD S WTR), Least Significant Byte 91 SDRAM Read to Precharge Command Delay (RTP, RTP sir), Least Significant Byte 92 SDRAM Read to Precharge Command Delay (RTP, RTP sir), Most Significant Byte 93 SDRAM Read to Precharge Command Delay (RTP, RTP sir), Lower Clock Limit 94 SDRAM Read to Read Command Delay (RTP, RTP sir), Lower Clock Limit 95 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (tCCD M), Least Significant Byte 96 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (tCCD M), Most Significant Byte 97 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (tCCD M), Most Significant Byte 98 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (tCCD M), Most Significant Byte 99 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M), Most Significant Byte 99 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M), WR), Least Significant Byte 99 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M) WR), Least Significant Byte 90 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M) WR), Least Significant Byte
SDRAM Write to Read Command Delay for Same Bank Group (ICCD L WTR), Most Significant Byte 85 SDRAM Write to Read Command Delay for Same Bank Group (ICCD L WTR), Most Significant Byte 87 SDRAM Write to Read Command Delay for Same Bank Group (ICCD L WTR), Most Significant Byte 88 SDRAM Write to Read Command Delay for Different Bank Group (ICCD S WTR), Loset Significant Byte 89 SDRAM Write to Read Command Delay for Different Bank Group (ICCD S WTR), Most Significant Byte 90 SDRAM Write to Read Command Delay for Different Bank Group, (ICCD S WTR), Loset Clock Limit 91 SDRAM Read to Precharge Command Delay (RTP, RTP sir), Loset Significant Byte 92 SDRAM Read to Precharge Command Delay (RTP, RTP sir), Loset Significant Byte 93 SDRAM Read to Precharge Command Delay (RTP, RTP sir), Loset Significant Byte 94 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (ICCD M), Least Significant Byte 95 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (ICCD M), Most Significant Byte 96 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (ICCD M), Most Significant Byte 97 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (ICCD M WR), Loset Significant Byte 98 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (ICCD M WR), Loset Significant Byte 98 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (ICCD M WR), Loset Significant Byte 99 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (ICCD M WR), Loset Significant Byte 99 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (ICCD M WR), Loset Significant Byte 90 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (ICCD M WR), Loset Significant Byte
SDRAM Write to Read Command Delay for Same Bank Group (tCCD L WTR), Most Significant Byte 87 SDRAM Write to Read Command Delay for Same Bank Group (tCCD L WTR), Loast Significant Byte 89 SDRAM Write to Read Command Delay for Different Bank Group (tCCD S WTR), Loast Significant Byte 89 SDRAM Write to Read Command Delay for Different Bank Group (tCCD S WTR), Most Significant Byte 90 SDRAM Write to Read Command Delay for Different Bank Group (tCCD S WTR), Most Significant Byte 91 SDRAM Read to Precharge Command Delay (tRTP, tRTP sir), Loast Significant Byte 92 SDRAM Read to Precharge Command Delay (tRTP, tRTP sir), Most Significant Byte 93 SDRAM Read to Precharge Command Delay (tRTP, tRTP sir), Lower Clock Limit 94 SDRAM Read to Precharge Command Delay (tRTP, tRTP sir), Lower Clock Limit 95 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (tCCD M), Most Significant Byte 96 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (tCCD M), Lower Clock Limit 97 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M), Lower Clock Limit 98 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M), Lower Clock Limit 99 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M), Lower Clock Limit 90 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M), WR), Loast Significant Byte 90 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M), WR), Loast Significant Byte 91 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M), WR), Loast Significant Byte
SDRAM Write to Read Command Delay for Same Bank Group (tCCD L WTR), Most Significant Byte 87 SDRAM Write to Read Command Delay for Same Bank Group (tCCD L WTR), Loast Significant Byte 89 SDRAM Write to Read Command Delay for Different Bank Group (tCCD S WTR), Loast Significant Byte 89 SDRAM Write to Read Command Delay for Different Bank Group (tCCD S WTR), Most Significant Byte 90 SDRAM Write to Read Command Delay for Different Bank Group (tCCD S WTR), Most Significant Byte 91 SDRAM Read to Precharge Command Delay (tRTP, tRTP sir), Loast Significant Byte 92 SDRAM Read to Precharge Command Delay (tRTP, tRTP sir), Most Significant Byte 93 SDRAM Read to Precharge Command Delay (tRTP, tRTP sir), Lower Clock Limit 94 SDRAM Read to Precharge Command Delay (tRTP, tRTP sir), Lower Clock Limit 95 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (tCCD M), Most Significant Byte 96 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (tCCD M), Lower Clock Limit 97 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M), Lower Clock Limit 98 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M), Lower Clock Limit 99 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M), Lower Clock Limit 90 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M), WR), Loast Significant Byte 90 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M), WR), Loast Significant Byte 91 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M), WR), Loast Significant Byte
SPRAM Write to Read Command Delay for Same Bank Group (tCCD L WTR), Loast Significant Byte SPRAM Write to Read Command Delay for Different Bank Group (tCCD S WTR), Loast Significant Byte SPRAM Write to Read Command Delay for Different Bank Group (tCCD S WTR), Most Significant Byte SPRAM Write to Read Command Delay for Different Bank Group (tCCD S WTR), Most Significant Byte SPRAM Read to Precharge Command Delay (tRTP, tRTP sir), Loast Significant Byte SPRAM Read to Precharge Command Delay (tRTP, tRTP sir), Most Significant Byte SPRAM Read to Precharge Command Delay (tRTP, tRTP sir), Lower Clock Limit SPRAM Read to Precharge Command Delay (tRTP, tRTP sir), Lower Clock Limit SPRAM Read to Read Command Delay (tRTP, tRTP sir), Lower Clock Limit SPRAM Read to Read Command Delay for Different Bank in Same Bank Group (tCCD M), Most Significant Byte SPRAM Read to Read Command Delay for Different Bank in Same Bank Group (tCCD M), Most Significant Byte SPRAM Read to Read Command Delay for Different Bank in Same Bank Group (tCCD M), Most Significant Byte SPRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M), Most Significant Byte SPRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M), WR), Most Significant Byte SPRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M), WR), Most Significant Byte
SDRAM Write to Read Command Delay for Different Bank Group (CCD S WTR), Least Significant Byte 90 SDRAM Write to Read Command Delay for Different Bank Group (CCD S WTR), Most Significant Byte 91 SDRAM Write to Read Command Delay for Different Bank Group, (CCD S WTR), Lower Clock Limit 92 SDRAM Read to Precharge Command Delay (RTP, RTP sir), Least Significant Byte 93 SDRAM Read to Precharge Command Delay (RTP, RTP sir), Most Significant Byte 94 SDRAM Read to Precharge Command Delay (RTP, RTP sir), Lower Clock Limit 95 SDRAM Read to Read Command Delay (RTP, RTP sir), Lower Clock Limit 96 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (CCD M), Most Significant Byte 97 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (CCD M), Lower Clock Limit 98 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (CCD M), Lower Clock Limit 99 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (CCD M), Lower Clock Limit 8 nCK 98 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (CCD M WR), Least Significant Byte 98 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (CCD M WR), Most Significant Byte 20000
SPRAM Write to Read Command Delay for Different Bank Group (ICCD S WTR), Most Significant Byte 90 SDRAM Write to Read Command Delay for Different Bank Group,(ICCD S WTR), Lower Clock Limit 91 SDRAM Read to Precharge Command Delay (IRTP, IRTP sir), Least Significant Byte 92 SDRAM Read to Precharge Command Delay (IRTP, IRTP sir), Most Significant Byte 93 SDRAM Read to Precharge Command Delay (IRTP, IRTP sir), Lower Clock Limit 94 SDRAM Read to Precharge Command Delay (IRTP, IRTP sir), Lower Clock Limit 95 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (ICCD M), Least Significant Byte 96 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (ICCD M), Lower Clock Limit 97 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (ICCD M), WR), Least Significant Byte 98 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (ICCD M WR), Most Significant Byte 20000 ps
SDRAM Write to Read Command Delay for Different Bank Group (ICCD S WTR), Most Significant Byte SDRAM Write to Read Command Delay for Different Bank Group (ICCD S WTR), Lower Clock Limit SDRAM Read to Precharge Command Delay (IRTP, IRTP sir), Least Significant Byte SDRAM Read to Precharge Command Delay (IRTP, IRTP sir), Most Significant Byte SDRAM Read to Precharge Command Delay (IRTP, IRTP sir), Lower Clock Limit SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (ICCD M), Least Significant Byte SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (ICCD M), Most Significant Byte SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (ICCD M), Least Significant Byte SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (ICCD M), Least Significant Byte SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (ICCD M), Least Significant Byte SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (ICCD M) WR), Least Significant Byte SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (ICCD M) WR), Most Significant Byte
90 SDRAM Write to Read Command Delay for Different Bank Group,(CCD S WTR), Lower Clock Limit 91 SDRAM Read to Precharge Command Delay (RTP, RTP sir), Least Significant Byte 92 SDRAM Read to Precharge Command Delay (RTP, RTP sir), Most Significant Byte 93 SDRAM Read to Precharge Command Delay (RTP, RTP sir), Lower Clock Limit 94 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (CCD M), Least Significant Byte 95 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (CCD M), Most Significant Byte 96 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (CCD M), Lower Clock Limit 97 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (CCD M WR), Least Significant Byte 98 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (CCD M WR), Most Significant Byte 99 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (CCD M WR), Most Significant Byte
91 SDRAM Read to Precharge Command Delay (RTP, RTP str), Least Significant Byte 92 SDRAM Read to Precharge Command Delay (RTP, RTP str), Most Significant Byte 93 SDRAM Read to Precharge Command Delay (RTP, RTP str), Lower Clock Limit 94 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (CCD M), Least Significant Byte 95 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (CCD M), Most Significant Byte 96 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (CCD M), Lower Clock Limit 97 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (CCD M WR), Most Significant Byte 98 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (CCD M WR), Most Significant Byte
92 SDRAM Read to Precharge Command Delay (RTP, RTP sir), Most Significant Byte 93 SDRAM Read to Precharge Command Delay (RTP, RTP sir), Lower Clock Limit 94 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (ICCD M),Least Significant Byte 95 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (ICCD M),Most Significant Byte 96 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (ICCD M),Lover Clock Limit 97 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (ICCD M WR),Least Significant Byte 98 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (ICCD M WR),Most Significant Byte
93 SDRAM Read to Precharge Command Delay (RTP, RTP sir), Most Significant Byte 93 SDRAM Read to Precharge Command Delay (RTP, RTP sir), Lower Clock Limit 94 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (tCCD M), Least Significant Byte 95 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (tCCD M), Most Significant Byte 96 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (tCCD M), Lower Clock Limit 97 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M WR), Least Significant Byte 98 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M WR), Most Significant Byte 98 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M WR), Most Significant Byte
94 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (tCCD M),Least Significant Byte 95 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (tCCD M),Most Significant Byte 96 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (tCCD M),Lower Clock Limit 97 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M WR),Least Significant Byte 98 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M WR),Most Significant Byte
94 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (tCCD M),Least Significant Byte 95 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (tCCD M),Most Significant Byte 96 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (tCCD M),Lower Clock Limit 8 nCK 97 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M WR),Least Significant Byte 98 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M WR),Most Significant Byte
95 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (tCCD M),Most Significant Byte 96 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (tCCD M),Lower Clock Limit 8 nCK 97 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M WR),Least Significant Byte 98 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M WR),Most Significant Byte
96 SDRAM Read to Read Command Delay for Different Bank in Same Bank Group (tCCD M)Lower Clock Limit 97 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M WR)Least Significant Byte 98 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M WR),Most Significant Byte 20000
97 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M. WR),Least Significant Byte 98 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (tCCD M. WR),Most Significant Byte
98 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (ICCD M. WR), Most Significant Byte 20000 ps
98 SDRAM Write to Write Command Delay for Different Bank in Same Bank Group (ICCD M. WR), Most Significant Byte
99 SUPON Write to write command belay for billierent Bank in Same Bank Group (ICCD IN WR); Lower Clock billit
100 SDRAM Write to Read Command Delay for Different Bank in Same Bank Group (ICCD M WTR)Least Significant Byte 10000 ps
101 SDRAM Write to Read Command Delay for Different Bank in Same Bank Group (ICCD M WTR), Most Significant Byte
102 SDRAM Write to Read Command Delay for Different Bank in Same Bank Group (ICCD M WTR) Lower Clock Limit 16 nCK
180-181
128-191 Reserved for future use Reserved for future use
192 SPD Revision for Module Information Version 1.1
193 Hashing Sequence No authentication
195 SPD Manufacturer ID Code, Second Byte
196 SPD Device Type
197 SPD Device Revision Number
By SPD Hub & PMIC Vendor & Revision
198 PMIC 0 Manufacturer ID Code, First Byte "Note: 1
199 PMIC 0 Manufacturer ID Code, Second Byte
133 a store a successorate on regular approprie plant
200 PMIC 0 Device Type
201 PMIC 0 Revision Number
202 PMIC 1 Manufacturer ID Code, First Byte
203 PMIC 1 Manufacturer ID Code, Second Byte
204 PMIC 1 Device Type
205 PMIC 1 Revision Number
206 PMIC 2 Manufacturer ID Code, First Byte
207 PMIC 2 Manufacturer ID Code, Second Byte
208 PMIC 2 Device Type
209 PMIC 2 Revision Number
209 PMIC 2 Revision Number 210 Thermal Sensor Manufacturer ID Code, First Byte
209 PMIC 2 Revision Number 210 Thermal Sensor Manufacturer ID Code, First Byte



2.10 Mineral Second Revision Number					
131	213	Thermal Sensor Revision Number			0
1915 PMCD Sepontation Level					0
151		·			0
AND Specification Level					0
218					0
299 Seperit reaction Level					0
200					0
Reserved Reserved Received					0
2300 Montanteering Medical Resistance Report Services 2 mm Tolonismos Foot 1 * Prof. 1 *			_		
2231 Abbustiment Meducia Maniform Priciness Review of Revi					0
2323 Abbustiment Reference Resident Seed Revision 0 Die 199 CT IncoRRMI					01
223	231	(Unbuffered): Module Maximum Thickness	Front,1 < thic	kness < 2 mm	0
1 Facis part	232	(Unbuffered): Reference Raw Card Used	Raw Card C	Revision 0	0:
200-2016 Reserved	233	(Unbuffered): DIMM Attributes	0 to +95 °C	/1 row DRAM	8
Missamed	234	(Unbuffered): Module Organization	1 Package Ran	ks/Per Channel	0
Reserved	235	Memory Channel Bus Width	2 channe	els/32 bits	2
44-600 Roseword for future use	236-239	Reserved	must be co	ded as 0x00	0
44-600 Roseword for future use			Res	erved	0
Description					0
Description					+ -
1512 Module Manufacturari Di Code, First Byle AdvanteCh					+
Module Manufacturing Dode, Sacond Byte			C	NO.	-
1513 Module Manufacturing Codes, Second Byte 1514 Module Manufacturing Codes Second Byte 1515 1516 1516 1516 1516 1516 1516 1517 1517 1518 1519			Adva	intech	8/
1515					С
516					
517 518 519 520 521 522 523 524 525 526 527 528 529 530 531 531 532 531 532 533 534 544 545 545 546 547 548	515	Module Manufacturing Date	"Note: 3	(Decimal)	
519	516	Module Manufacturing Date	"Note: 4	(Decimal)	
Social Number Note: 5 (Sectimal) Note: 5 (Sectimal)	517				
550 521 522 523 524 525 526 527 528 529 530 531 531 532 533 534 535 536 536 537 538 539 540 541 542 543 544 545 546 546 546 546 546	518				
521 522 523 524 525 526 527 528 529 530 531 531 532 533 534 535 536 537 538 539 540 541 542 543 544 544 545 546 547 548	519	Module Serial Number	*Note: 5	(Decimal)	
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528 529 530 531 532 533 533 534 536 536 538 539 540 540 542 543 544 545 545 546 547 548					
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532 533 534 Module Part Number *Note: 6 *Note: 6 *Note: 6 *Note: 6 537 538 539 540 541 542 543 544 545 546 546 547 548 549	530				
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536 537 538 539 540 541 542 543 544 544 545 546 547 548 549					
536 Module Part Number 537 538 539 540 541 542 543 544 545 546 546 547 548 549					\vdash
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541 542 543 544 545 546 547 548 549 550					L
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550					<u> </u>
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551 Module Revision Code					<u> </u>
	551	Module Revision Code			0
552 DRAM Manufacturer ID Code, First Byte Samsung	552	DRAM Manufacturer ID Code, First Byte	Cam	isling	8
553 DRAM Manufacturer ID Code, Second Byte Samsung	553	DRAM Manufacturer ID Code, Second Byte	San	and the same of	CI
554 DRAM Stepping	554	DRAM Stepping			9



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555-639	Manufacturer's Specific Data	*Note: 7	-
640	Intel Extreme Memory Profile Identification String		00
641	Intel Extreme Memory Profile Identification String		00
642	Intel Extreme Memory Profile Version		00
643	Intel Extreme Memory Profile Organization		00
644	Intel Extreme Memory Profile Configuration		00
	PMIC Vendor ID	-	00
	PMIC Vendor ID		00
	Number of PMICs		00
648	PMIC Capabilities		00
849-863			00
	ROYU		00
654			
655			00
656			00
657			00
658			00
659	第 3 頁		00
660			00
661	Profile 1 String Name		00
662	Tourism 1 serving 1 serving		00
663			00
664			00
665			00
666			00
667			00
668			00
669			00
670			00
671			00
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672			
673			00
674			00
675			00
676			00
677	Profile 2 String Name		00
678			00
679			00
680			00
681			00
682			00
683			00
684			00
685			00
686			00
687			00
688			00
			00
689			
690			00
691			00
692			00
693	Profile 3 String Name		00
694			00
695			00
696			00
697			00
698			00
699			00
700			00
701			00
	Cyclical Redundancy Code (CRC) for Base Configuration Section, Least Significant Byte (for bytes 640-701)		00
	Cyclical Redundancy Code (CRC) for Base Configuration Section, Most Significant Byte (for bytes 640–701)		00
703	Cyclical Redundancy Code (CRC) for Base Configuration Section, Most significant Byte (for bytes 640-701) Profile 1: Module VPP Voltage Level		00
	Module VDD Voltage Level		00
/ (05	MODULE YEAR YORKING LEVEL		00



706	Module VDDQ Voltage Level	l	r on
706	Module YDDG Voltage Level - THIS BYTE IS CURRENTLY RSVD		00
708	Memory Controller Voltage Level		00
709	SDRAM Minimum Cycle Time (tCKAVGmin),Least Significant Byte		00
710	SDRAM Minimum Cycle Time (tCKAVGmin) Most Significant Byte		00
711	SDRAM CAS Latencies Supported, First Byte		00
712	SDRAM CAS Latencies Supported,Second Byte		00
713	SDRAM CAS Latencies Supported, Third Byte		00
714	SDRAM CAS Latencies Supported, Fourth Byte		00
715	SDRAM CAS Latencies Supported,Fifth Byte		00
716	RSVD for future CAS Latency		00
717	SDRAM Minimum CAS Latency Time (tAAmin),Least Significant Byte		00
718	SDRAM Minimum CAS Latency Time (kAAmin),Most Significant Byte		00
719	SDRAM Minimum RAS to CAS Delay Time (RCDmin),Least Significant Byte		00
720	SDRAM Minimum RAS to CAS Delay Time (tRCDmin),Most Significant Byte		00
721	SDRAM Minimum Row Precharge Delay Time (tRPmin),Least Significant Byte		00
722	SDRAM Minimum Row Precharge Delay Time (RPmin),Most Significant Byte		00
723	SDRAM Minimum Active to Precharge Delay Time (tRASmin),Least Significant Byte		00
724	SDRAM Minimum Active to Precharge Delay Time (tRASmin),Most Significant Byte		00
725	SDRAM Minimum Active to Active/Refresh Delay Time(tRCmin) ,Least Significant Byte		00
726	SDRAM Minimum Active to Active/Refresh Delay Time(tRCmin) ,Most Significant Byte		00
727	SDRAM Minimum Write Recovery Time (tWRmin),Least Significant Byte		00
728	SDRAM Minimum Write Recovery Time (tWRmin),Most Significant Byte		00
729	SDRAM Minimum Refresh Recovery Delay Time(tRPC1min),Least Significant Byte		00
730	SDRAM Minimum Refresh Recovery Delay Time(RFC1min),Most Significant Byte		00
731	SDRAM Minimum Refresh Recovery Delay Time(tRPC2min),Least Significant Byte		00
732	SDRAM Minimum Refresh Recovery Delay Time(RFC2min),Most Significant Byte		00
733	SDRAM Minimum Refresh Recovery Delay Time(RFCsb),Least Significant Byte		00
734	SDRAM Minimum Refresh Recovery Delay Time(tRFCsbmin),Most Significant Byte		00
735-762	RSVD,must be coded as 0x00		00
763 764	Advanced Memory Overclocking Features System CMD Rate Mode		00
765	Vendor Personality Byte - RSVD		00
766	Cyclical Redundancy Code (CRC) for Base Configuration Section, Least Significant Byte(for bytes 704–765)		00
767	Cyclical Redundancy Code (CRC) for Base Configuration Section, Most Significant Byte(for bytes 704-765)		00
768	Profile2: Module VPP Voltage Level		00
769	Module VDD Voltage Level		00
770	Module VDDQ Voltage Level		00
771	Module TBD Voltage Level - THIS BYTE IS CURRENTLY RSVD		00
772	Memory Controller Voltage Level		00
773	SDRAM Minimum Cycle Time (tCKAVGmin)Least Significant Byte		00
774	SDRAM Minimum Cycle Time (tCKAVGmin) Most Significant Byte		00
775	SDRAM CAS Latencies Supported,First Byte		00
776	SDRAM CAS Latencies Supported,Second Byte		00
777	SDRAM CAS Latencies Supported, Third Byte		00
778	SDRAM CAS Latencies Supported,Fourth Byte		00
779	SDRAM CAS Latencies Supported,Fifth Byte		00
780	RSVD for future CAS Latency		00
781	SDRAM Minimum CAS Latency Time (tAAmin),Least Significant Byte		00
782	SDRAM Minimum CAS Latency Time (tAAmin),Most Significant Byte		00
783	SDRAM Minimum RAS to CAS Delay Time (tRCDmin),Least Significant Byte		00
784	SDRAM Minimum RAS to CAS Delay Time (RCDmin),Most Significant Byte		00
785	SDRAM Minimum Row Precharge Delay Time (RPmin),Least Significant Byte		00
786	SDRAM Minimum Row Precharge Delay Time (IRPmin),Most Significant Byte		00
787	SDRAM Minimum Active to Precharge Delay Time (tRASmin),Least Significant Byte		00
788	SDRAM Minimum Active to Precharge Delay Time (BASmin),Most Significant Byte		00
789	SDRAM Minimum Active to Active/Refresh Delay Time(tRCmin) ,Least Significant Byte		00
790	SDRAM Minimum Active to Active/Refresh Delay Time(tRCmin) ,Most Significant Byte		00
791	SDRAM Minimum Write Recovery Time (tWRmin),Least Significant Byte		00
792	SDRAM Minimum Write Recovery Time (tWRmin),Most Significant Byte		00
793	SDRAM Minimum Refresh Recovery Delay Time(RFC1min),Least Significant Byte		00
794	SDRAM Minimum Refresh Recovery Delay Time(RFC1min),Most Significant Byte		00
795	SDRAM Minimum Refresh Recovery Delay Time(tRFC2min),Least Significant Byte		00
	SDRAM Minimum Refresh Recovery Delay Timet/RFC2min1Most Significant Byte		



262Pin DDR5 5600 1.1V SO-DIMM 8GB Based on 1024Mx16 AQD-SD5V8GN56-SC

Table				
SYSTO-must be cooled as Drift	797	SDRAM Minimum Refresh Recovery Delay Time(RPCsb),Least Significant Byte		00
Avanced Memory, Overticoking Reduces 9 System Composition State Mode 9 System Composition State Mode 9 Vertical Reductancy Code (CRC) for Base Configuration Section, Least Significant Bytefor bytes 769–829) 90 Vertical Reductancy Code (CRC) for Base Configuration Section, Most Significant Bytefor bytes 769–829) 91 Vertical Reductancy Code (CRC) for Base Configuration Section, Most Significant Bytefor bytes 769–829) 92 Vertical Reductancy Code (CRC) for Base Configuration Section, Most Significant Bytefor bytes 769–829) 93 Vertical Reductancy Code (CRC) for Base Configuration Section, Most Significant Bytefor Bytes Section S	798	SDRAM Minimum Refresh Recovery Delay Time(RFCsbmin),Most Significant Byte		00
Septembroad	799-826	RSVD,must be coded as 0x00		00
Accordance Processing Byte Accordance	827	Advanced Memory Overclocking Features		00
STORY Continued Resolutionary Code (CRC) to Base Configura Bon Section, Most Significant Byte/for bytes 766-929) Story Continued Resolutionary Code (CRC) to Base Configura Bon Section, Most Significant Byte/for bytes 766-929) Story Continued Resolution Res	828	System CMD Rate Mode		00
SPANDA CAS Litancies Supported Froit Byte	829	Vendor Personality Byte - RSVD		00
### Potrices Absolute VEPP Voltage Level ### Modale VEDOL VED	830	Cyclical Redundancy Code (CRC) for Base Configura tion Section, Least Significant Byte(for bytes 768–829)		00
Module VED Voltage Level Module VED Voltage Level Module TED Voltage Level Module TED Voltage Level - THES BYTE IS CURRENTLY RSVD Module TED Voltage Level - THES BYTE IS CURRENTLY RSVD Module TED Voltage Level - THES BYTE IS CURRENTLY RSVD Module TED Voltage Level - THES BYTE IS CURRENTLY RSVD Module TED Voltage Level - THES BYTE IS CURRENTLY RSVD Module TED Voltage Level - THES BYTE IS CURRENTLY RSVD Module TED Voltage Level - THE BYTE IS CURRENTLY RSVD Module TED Voltage Level - THE MODULE	831	Cyclical Redundancy Code (CRC) for Base Configura tion Section, Most Significant Byte(for bytes 768–829)		00
Mondar YDO Violage Level - THIS BYTE IS CURRENTLY RSVD	832	Profile3 :Module VPP Voltage Level		00
Models TBD Visitiops Level - THIS BYTE IS CURRENTLY RSVD Models TBD Visitiops Level - THIS BYTE IS CURRENTLY RSVD Minimum Cycle Time (DCAAVGmin) Lasts Significant Byte Minimum Cycle Latencies Supported. First Byte Minimum Cycle Latencies Supported. First Byte Minimum CAS Latencies Cas Latencies Significant Byte Minimum CAS Latencies	833	Module VDD Voltage Level		00
Memory Controller Violage Level ST SDRAM Minimum Cycle Time (BCKAVGmin) Lleast Significant Byte SSRAM Minimum Cycle Time (BCKAVGmin) Lleast Significant Byte SSRAM CAS Latencies Supported, Second Byte SSRAM Minimum CAS Latency Time (BACHINI) Lleast Significant Byte SSRAM Minimum CAS Latency Time (BACHINI) Lleast Significant Byte SSRAM Minimum CAS Latency Time (BACHINI) Lleast Significant Byte SSRAM Minimum CAS Latency Time (BACHINI) Lleast Significant Byte SSRAM Minimum RAS to CAS Dolay Time (SPCDIMI) Lleast Significant Byte SSRAM Minimum RAS to CAS Dolay Time (SPCDIMI) Lleast Significant Byte SSRAM Minimum Rose Peachage Dolay Time (SPCDIMI) Lleast Significant Byte SSRAM Minimum Rose Peachage Dolay Time (SPCSIMI) Lleast Significant Byte SSRAM Minimum Rose Peachage Dolay Time (SPASIMI) Lleast Significant Byte SSRAM Minimum Active to Active/Refered Dolay Time (SPASIMI) Lleast Significant Byte SSRAM Minimum Active to Prechage Dolay Time (SPASIMI) Lleast Significant Byte SSRAM Minimum Refere Recovery Dolay Time (SPASIMI) Lleast Significant Byte SSRAM Minimum Refere Recovery Dolay Time (SPASIMI) Lleast Significant Byte SSRAM Minimum Refere Recovery Dolay Time (SPASIMI) Lleast Significant Byte SSRAM Minimum Refere Recovery Dolay Time(SPRCTIMI) Lleast Significant Byte SSRAM Minimum Refere Recovery Dolay Time(SPRCTIMI) Lleast Significant Byte SSRAM Minimum Refere Recovery Dolay Time(SPRCTIMI) Lleast Significant Byte SSRAM Minimum Refere Recovery Dolay Time(SPRCTIMI) Lleast Significant Byte SSRAM Minimum Refere Recovery Dola	834	Module VDDQ Voltage Level		00
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SCRAM CAS Latencies Supported. First Byte 504 507AM CAS Latencies Supported. Second Byte 605 507AM CAS Latencies Supported. There Byte 606 507AM CAS Latencies Supported. There Byte 607 507AM CAS Latencies Supported. There Byte 607 507AM ACT CAS Latencies Supported. There Byte 607 507AM Marinium CAS Latency 507AM Marinium CAS Latency 507AM Marinium CAS Latency 507AM Marinium CAS Latency Time (MArmin) Least Significant Byte 607AM Marinium CAS Latency 507AM Marinium CAS Latency Time (MArmin) Least Significant Byte 608 507AM Marinium RAS to CAS Delay Time (MCComin) Least Significant Byte 609 507AM Marinium Row Precharge Delay Time (MCComin) Least Significant Byte 600 507AM Marinium Row Precharge Delay Time (MCComin) Least Significant Byte 600 507AM Marinium Row Precharge Delay Time (MCComin) Least Significant Byte 600 507AM Marinium Row Precharge Delay Time (MCComin) Least Significant Byte 600 507AM Marinium Active to Precharge Delay Time (MCComin) Least Significant Byte 600 507AM Marinium Active to Precharge Delay Time (MCComin) Least Significant Byte 600 507AM Marinium Active to Precharge Delay Time (MCComin) Least Significant Byte 600 507AM Marinium Active to Precharge Delay Time (MCComin) Least Significant Byte 600 507AM Marinium Active to Active Markens Delay Time (MCComin) Least Significant Byte 600 507AM Marinium Marinium Row Precharge Delay Time (MCComin) Least Significant Byte 600 507AM Marinium Row Row Precharge Delay Time (MCComin) Least Significant Byte 600 507AM Marinium Row Row Rowery Delay Time (MCComin) Least Significant Byte 601 507AM Marinium Row Rowery Delay Time (MCComin) Least Significant Byte 602 507AM Marinium Row Rowery Delay Time (MCComin) Least Significant Byte 603 507AM Marinium Rower Rowery Delay Time (MCComin) Least Significant Byte 604 505AW SERVIN Marinium Rower Rowery Delay Time (MCComin) Least Significant Byte 605 507AM Marinium Rower Rowery Delay Time (MCComin) Least Significant Byte 606 507AW Marinium Rower Rowery Delay Time (837	SDRAM Minimum Cycle Time (tCKAVGmin),Least Significant Byte		00
SPRAM CAS Latencies Supported, Second Byte 61 61 61 61 61 61 61 61 61 6	838	SDRAM Minimum Cycle Time (tCKAVGmin),Most Significant Byte		8
B41 SDRAM CAS Labencies Supported, Third Byte 505 505 505 505 505 505 505 5	839	SDRAM CAS Latencies Supported, First Byte		00
SPAM CAS Latencies Supported, Fourth Byte SORAM CAS Latencies Supported, Front Byte OR SORAM CAS Latencies Supported, Front Byte OR SORAM Minimum CAS Latency Time (MAmin), Least Significant Byte SORAM Minimum CAS Latency Time (MAmin), Least Significant Byte OR SORAM Minimum RAS to CAS Delay Time (MAmin), Least Significant Byte OR SORAM Minimum RAS to CAS Delay Time (RCOmin), Least Significant Byte SORAM Minimum RAS to CAS Delay Time (RCOmin), Least Significant Byte SORAM Minimum Row Precharge Delay Time (RPInim), Least Significant Byte SORAM Minimum Row Precharge Delay Time (RPInim), Least Significant Byte SORAM Minimum Active to Precharge Delay Time (RPInim), Least Significant Byte SORAM Minimum Active to Precharge Delay Time (RPInim), Least Significant Byte SORAM Minimum Active to Precharge Delay Time (RPInim), Least Significant Byte SORAM Minimum Active to Precharge Delay Time (RPInim), Least Significant Byte SORAM Minimum Active to Precharge Delay Time (RPInim), Least Significant Byte SORAM Minimum Active to Active/Refresh Delay Time(RPInim), Least Significant Byte SORAM Minimum Minimum Active to Active/Refresh Delay Time(RPInim), Least Significant Byte SORAM Minimum Refresh Recovery Time (RVRimin), Least Significant Byte SORAM Minimum Refresh Recovery Delay Time(RVRimin), Least Significant Byte SORAM Minimum Refresh Recovery Delay Time(RVRImin), Least Significant Byte SORAM Minimum Refresh Recovery Delay Time(RVRImin), Least Significant Byte SORAM Minimum Refresh Recovery Delay Time(RVRImin), Least Significant Byte SORAM Minimum Refresh Recovery Delay Time(RVRImin), Least Significant Byte SORAM Minimum Refresh Recovery Delay Time(RVRImin), Least Significant Byte SORAM Minimum Refresh Recovery Delay Time(RVRImin), Least Significant Byte SORAM Minimum Refresh Recovery Delay Time(RVRImin), Least Significant Byte SORAM Minimum Refresh Recovery Delay Time(RVRImin), Least Significant Byte SORAM Minimum Refresh Recovery Delay Time(RVRImin), Least Significant Byte SORAM Minimum Refr	840	SDRAM CAS Latencies Supported,Second Byte		00
843 SDRAM CAS Latencies Supported Fifth Byte 844 RSVD for future CAS Latency Time (MArtin) Least Significant Byte 955 SDRAM Minimum CAS Latency Time (MArtin) Least Significant Byte 965 SDRAM Minimum CAS Latency Time (MArtin) Least Significant Byte 966 SDRAM Minimum RAS to CAS Delay Time (RECDmin) Least Significant Byte 967 SDRAM Minimum RAS to CAS Delay Time (RECDmin) Least Significant Byte 968 SDRAM Minimum Row Precharge Delay Time (REPmin) Least Significant Byte 969 SDRAM Minimum Row Precharge Delay Time (REPmin) Least Significant Byte 960 SDRAM Minimum Row Precharge Delay Time (REPmin) Least Significant Byte 960 SDRAM Minimum Active to Precharge Delay Time (REPmin) Least Significant Byte 961 SDRAM Minimum Active to Precharge Delay Time (REPmin) Least Significant Byte 962 SDRAM Minimum Active to Precharge Delay Time (REPmin) Least Significant Byte 963 SDRAM Minimum Active to Precharge Delay Time (REPmin) Least Significant Byte 964 SDRAM Minimum Active to Active Refereb Delay Time (REPmin) Least Significant Byte 965 SDRAM Minimum Active to Active Refereb Delay Time (REPmin) Least Significant Byte 966 SDRAM Minimum With Recovery Time (WRImin) Least Significant Byte 967 SDRAM Minimum Refereb Recovery Delay Time(REPCDI) Least Significant Byte 968 SDRAM Minimum Refereb Recovery Delay Time(REPCDI) Least Significant Byte 969 SDRAM Minimum Refereb Recovery Delay Time(REPCDI) Least Significant Byte 960 SDRAM Minimum Refereb Recovery Delay Time(REPCDI) Least Significant Byte 961 SDRAM Minimum Refereb Recovery Delay Time(REPCDI) Least Significant Byte 962 SDRAM Minimum Refereb Recovery Delay Time(REPCDI) Least Significant Byte 963 SDRAM Minimum Refereb Recovery Delay Time(REPCDI) Least Significant Byte 964 SDRAM Minimum Refereb Recovery Delay Time(REPCDI) Least Significant Byte 965 SDRAM Minimum Refereb Recovery Delay Time(REPCDI) Least Significant Byte 966 SDRAM Minimum Refereb Recovery Delay Time(REPCDI) Least Significant Byte 967 SDRAM Minimum Refereb Recovery Delay Time(REPCDI) Least Significant Byte 968 SDRAM Minim	841	SDRAM CAS Latencies Supported, Third Byte		00
RSVD for future CAS Latency SCRAM Minimum CAS Latency Time (RAmin) Least Significant Byte SCRAM Minimum CAS Latency Time (RACDmin) Least Significant Byte SCRAM Minimum RAS to CAS Delay Time (RCDmin) Least Significant Byte SCRAM Minimum RAS to CAS Delay Time (RCDmin) Least Significant Byte SCRAM Minimum RAS to CAS Delay Time (RCDmin) Least Significant Byte SCRAM Minimum RAS to CAS Delay Time (RCDmin) Least Significant Byte SCRAM Minimum RAS to CAS Delay Time (RCDmin) Least Significant Byte SCRAM Minimum Row Precharge Delay Time (RPCmin) Least Significant Byte SCRAM Minimum Active to Precharge Delay Time (RPCmin) Least Significant Byte SCRAM Minimum Active to Precharge Delay Time (RASmin) Least Significant Byte SCRAM Minimum Active to Precharge Delay Time (RASmin) Least Significant Byte SCRAM Minimum Active to Active/Refresh Delay Time(RRCmin) Least Significant Byte SCRAM Minimum Active to Active/Refresh Delay Time(RRCmin) Least Significant Byte SCRAM Minimum Wirtle Recovery Time (WRimin) Least Significant Byte SCRAM Minimum Wirtle Recovery Time (WRImin) Least Significant Byte SCRAM Minimum Refresh Recovery Delay Time(RRCTmin) Least Significant Byte SCRAM Minimum Refresh Recovery Delay Time(RRCTmin) Least Significant Byte SCRAM Minimum Refresh Recovery Delay Time(RRCTmin) Least Significant Byte SCRAM Minimum Refresh Recovery Delay Time(RRCTmin) Least Significant Byte SCRAM Minimum Refresh Recovery Delay Time(RRCTmin) Least Significant Byte SCRAM Minimum Refresh Recovery Delay Time(RRCTmin) Least Significant Byte SCRAM Minimum Refresh Recovery Delay Time(RRCTmin) Least Significant Byte SCRAM Minimum Refresh Recovery Delay Time(RRCTmin) Least Significant Byte SCRAM Minimum Refresh Recovery Delay Time(RRCTmin) Least Significant Byte SCRAM Minimum Refresh Recovery Delay Time(RRCTmin) Least Significant Byte SCRAM Minimum Refresh Recovery Delay Time(RRCTmin) Least Significant Byte SCRAM Minimum Refresh Recovery Delay Time(RRCTmin) Least Significant Byte SCRAM Minimum Refresh Recovery Delay Time(RRCTmin) Least Significa	842	SDRAM CAS Latencies Supported,Fourth Byte		00
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848 SDRAM Minimum RAS to CAS Delay Time (RPCmin),Most Significant Byte 850 SDRAM Minimum Row Precharge Delay Time (RPPmin),Loast Significant Byte 851 SDRAM Minimum Row Precharge Delay Time (RPPmin),Loast Significant Byte 852 SDRAM Minimum Active to Precharge Delay Time (RRASmin),Loast Significant Byte 853 SDRAM Minimum Active to Precharge Delay Time (RRASmin),Most Significant Byte 854 SDRAM Minimum Active to Active/Refresh Delay Time(RCmin), Loast Significant Byte 855 SDRAM Minimum Active to Active/Refresh Delay Time(RCmin), Most Significant Byte 866 SDRAM Minimum Write Recovery Time (WRMin),Most Significant Byte 867 SDRAM Minimum Write Recovery Time (WRMin),Most Significant Byte 868 SDRAM Minimum Refresh Recovery Delay Time(RPCmin),Most Significant Byte 869 SDRAM Minimum Refresh Recovery Delay Time(RPCmin),Most Significant Byte 860 SDRAM Minimum Refresh Recovery Delay Time(RPCmin),Most Significant Byte 861 SDRAM Minimum Refresh Recovery Delay Time(RPCmin),Most Significant Byte 862 SDRAM Minimum Refresh Recovery Delay Time(RPCCmin),Most Significant Byte 863 SDRAM Minimum Refresh Recovery Delay Time(RPCCmin),Most Significant Byte 864 SDRAM Minimum Refresh Recovery Delay Time(RPCCmin),Most Significant Byte 865 SDRAM Minimum Refresh Recovery Delay Time(RPCCmin),Most Significant Byte 866 SDRAM Minimum Refresh Recovery Delay Time(RPCCmin),Most Significant Byte 867 SDRAM Minimum Refresh Recovery Delay Time(RPCCmin),Most Significant Byte 868 SDRAM Minimum Refresh Recovery Delay Time(RPCCmin),Most Significant Byte 869 SDRAM Minimum Refresh Recovery Delay Time(RPCCmin),Most Significant Byte 860 SDRAM Minimum Refresh Recovery Delay Time(RPCCmin),Most Significant Byte 861 SDRAM Minimum Refresh Recovery Delay Time(RPCCmin),Most Significant Byte 862 SDRAM Minimum Refresh Recovery Delay Time(RPCCmin),Most Significant Byte 863 SDRAM Minimum Refresh Recovery Delay Time(RPCCmin),Most Significant Byte 864 SQL Refresh Recovery Delay Time(RPCCmin),Most Significant Byte 865 SDRAM Minimum Refresh Recovery Delay Time(RPCCmin),Most Si	846	SDRAM Minimum CAS Latency Time (tAAmin),Most Significant Byte		00
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851 SDRAM Minimum Active to Precharge Delay Time (RASmin) Least Significant Byte 852 SDRAM Minimum Active to Active Referesh Delay Time (RASmin) Most Significant Byte 853 SDRAM Minimum Active to Active Referesh Delay Time (RASmin) Most Significant Byte 854 SDRAM Minimum Write Recovery Time (WRmin) Least Significant Byte 855 SDRAM Minimum Write Recovery Time (WRmin) Most Significant Byte 856 SDRAM Minimum Write Recovery Time (WRmin) Most Significant Byte 857 SDRAM Minimum Refresh Recovery Delay Time(RFC1min) Least Significant Byte 858 SDRAM Minimum Refresh Recovery Delay Time(RFC1min) Least Significant Byte 859 SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte 860 SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte 861 SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte 862 SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte 863 SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte 864 SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte 865 SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte 866 SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte 867 SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte 868 SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte 869 SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte 870 SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Bytefor bytes 832–893) 870 October Personality Byte - RSVD 870 October Redundancy Code (CRC) for Base Configura tion Section, Most Significant Bytefor bytes 832–893) 870 October Redundancy Code (CRC) for Base Configura tion Section, Most Significant Bytefor bytes 832–893)	849	SDRAM Minimum Row Precharge Delay Time (RPmin),Least Significant Byte		00
SDRAM Minimum Active to Active/Refresh Delay Time (RASmin) Most Significant Byte 853 SDRAM Minimum Active to Active/Refresh Delay Time(RCmin) Least Significant Byte 854 SDRAM Minimum Active to Active/Refresh Delay Time(RCmin) Most Significant Byte 855 SDRAM Minimum Write Recovery Time (WRmin) Most Significant Byte 856 SDRAM Minimum Write Recovery Time (WRmin) Most Significant Byte 857 SDRAM Minimum Refresh Recovery Delay Time(RFC1min) Least Significant Byte 858 SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Least Significant Byte 859 SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Least Significant Byte 860 SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Least Significant Byte 861 SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte 862 SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte 863 SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte 864 SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte 865 SDRAM Minimum Refresh Recovery Delay Time(RFCabin) Most Significant Byte 866 SDRAM Minimum Refresh Recovery Delay Time(RFCabin) Most Significant Byte 867 SDRAM Minimum Refresh Recovery Delay Time(RFCabin) Most Significant Byte 868 SDRAM Minimum Refresh Recovery Delay Time(RFCabin) Most Significant Byte 869 SDRAM Minimum Refresh Recovery Delay Time(RFCabin) Most Significant Byte 860 SDRAM Minimum Refresh Recovery Delay Time(RFCabin) Most Significant Byte 861 SDRAM Minimum Refresh Recovery Delay Time(RFCabin) Most Significant Byte 862 SDRAM Minimum Refresh Recovery Delay Time(RFCabin) Most Significant Byte 863 Vendor Personality Byte - RSVD 864 Cyclical Redundancy Code (CRC) for Base Configura tion Section, Most Significant Byte(for bytes 832–893) 865 Cyclical Redundancy Code (CRC) for Base Configura tion Section, Most Significant Byte(for bytes 832–893)	850	SDRAM Minimum Row Precharge Delay Time (RPmin),Most Significant Byte		00
SDRAM Minimum Active to Active/Refresh Delay Time(RCmin) Least Significant Byte 854 SDRAM Minimum Write Recovery Time (WRmin) Least Significant Byte 855 SDRAM Minimum Write Recovery Time (WRmin) Least Significant Byte 856 SDRAM Minimum Write Recovery Time (WRmin) Least Significant Byte 857 SDRAM Minimum Refresh Recovery Delay Time(RFC1min) Least Significant Byte 858 SDRAM Minimum Refresh Recovery Delay Time(RFC1min) Least Significant Byte 859 SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte 860 SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte 861 SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte 862 SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte 863 SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte 864 SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte 865 SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte 866 SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte 867 SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte 868 SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte 869 SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte 860 SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte 861 SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte(for bytes 832-893) 862 SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte(for bytes 832-893) 863 Vendor Personality Byte - RSVD 864 Cyclical Redundancy Code (CRC) for Base Configura tion Section, Most Significant Byte(for bytes 832-893)	851	SDRAM Minimum Active to Precharge Delay Time (RASmin),Least Significant Byte		00
SDRAM Minimum Active to Active/Refresh Delay Time(RCmin) Most Significant Byte 855 SDRAM Minimum Write Recovery Time (tWRmin) Least Significant Byte 856 SDRAM Minimum Write Recovery Time (tWRmin) Least Significant Byte 857 SDRAM Minimum Refresh Recovery Delay Time(RFC-Imin) Least Significant Byte 858 SDRAM Minimum Refresh Recovery Delay Time(RFC-Imin) Least Significant Byte 859 SDRAM Minimum Refresh Recovery Delay Time(RFC-Imin) Least Significant Byte 860 SDRAM Minimum Refresh Recovery Delay Time(RFC-Imin) Least Significant Byte 861 SDRAM Minimum Refresh Recovery Delay Time(RFC-Imin) Most Significant Byte 862 SDRAM Minimum Refresh Recovery Delay Time(RFC-Sb) Least Significant Byte 863 RSVD, must be coded as 0x.00 864 Advanced Memory Overclocking Features 875 System CMD Rate Mode 875 System CMD Rate Mode 875 System CMD Rate Mode 876 Cyclical Redundancy Code (CRC) for Base Configura tion Section, Least Significant Byte(for bytes 832-893) 877 System CMD Rate Mode 877 System CMD Rate Mode 878 Cyclical Redundancy Code (CRC) for Base Configura tion Section, Most Significant Byte(for bytes 832-893)	852	SDRAM Minimum Active to Precharge Delay Time (tRASmin),Most Significant Byte		00
SDRAM Minimum Write Recovery Time (tWRmin),Most Significant Byte 856 SDRAM Minimum Refresh Recovery Delay Time(RFCImin),Loast Significant Byte 857 SDRAM Minimum Refresh Recovery Delay Time(RFCImin),Loast Significant Byte 858 SDRAM Minimum Refresh Recovery Delay Time(RFCImin),Most Significant Byte 859 SDRAM Minimum Refresh Recovery Delay Time(RFCImin),Most Significant Byte 860 SDRAM Minimum Refresh Recovery Delay Time(RFCImin),Most Significant Byte 861 SDRAM Minimum Refresh Recovery Delay Time(RFCImin),Most Significant Byte 862 SDRAM Minimum Refresh Recovery Delay Time(RFCImin),Most Significant Byte 863 RSVD,must be coded as 0x.00 864 Advanced Memory Overclocking Features 875 System CMD Rate Mode 875 System CMD Rate Mode 875 System CMD Rate Mode 875 Cyclical Redundancy Code (CRC) for Base Configura tion Section, Least Significant Byte(for bytes 832–893) 875 Cyclical Redundancy Code (CRC) for Base Configura tion Section, Most Significant Byte(for bytes 832–893)	853	SDRAM Minimum Active to Active/Refresh Delay Time(RCmin) ,Least Significant Byte		00
856 SDRAM Minimum Write Recovery Time (WRmin),Most Significant Byte 857 SDRAM Minimum Refresh Recovery Delay Time(RFC1min),Least Significant Byte 858 SDRAM Minimum Refresh Recovery Delay Time(RFC2min),Least Significant Byte 859 SDRAM Minimum Refresh Recovery Delay Time(RFC2min),Least Significant Byte 860 SDRAM Minimum Refresh Recovery Delay Time(RFC2min),Least Significant Byte 861 SDRAM Minimum Refresh Recovery Delay Time(RFC2min),Most Significant Byte 862 SDRAM Minimum Refresh Recovery Delay Time(RFCsbmin),Most Significant Byte 863 RSVD,must be coded as 0x00 864 Advanced Memory Overciocking Features 865 System CMD Rate Mode 867 System CMD Rate Mode 868 Cyclical Redundancy Code (CRC) for Base Configura tion Section, Least Significant Byte(for bytes 832-893) 869 Cyclical Redundancy Code (CRC) for Base Configura tion Section, Most Significant Byte(for bytes 832-893)	854	SDRAM Minimum Active to Active/Refresh Delay Time(RCmin) ,Most Significant Byte		00
SDRAM Minimum Refresh Recovery Delay Time(RFC1min)_Least Significant Byte	855	SDRAM Minimum Write Recovery Time (WRmin),Least Significant Byte		00
858 SDRAM Minimum Refresh Recovery Delay Time(RFC1min),Most Significant Byte 859 SDRAM Minimum Refresh Recovery Delay Time(RFC2min),Least Significant Byte 860 SDRAM Minimum Refresh Recovery Delay Time(RFC2min),Most Significant Byte 861 SDRAM Minimum Refresh Recovery Delay Time(RFCsb),Least Significant Byte 862 SDRAM Minimum Refresh Recovery Delay Time(RFCsb),Least Significant Byte 863 RSVD,must be coded as 0x00 861 Advanced Memory Overclocking Features 892 System CMD Rate Mode 893 Vendor Personality Byte - RSVD 894 Vendor Personality Byte - RSVD 895 Cyclical Redundancy Code (CRC) for Base Configura tion Section, Most Significant Byte(for bytes 832–893) 895 Cyclical Redundancy Code (CRC) for Base Configura tion Section, Most Significant Byte(for bytes 832–893)	856	SDRAM Minimum Write Recovery Time (tWRmin),Most Significant Byte		00
SDRAM Minimum Refresh Recovery Delay Time(RFC2min),Least Significant Byte OC	857	SDRAM Minimum Refresh Recovery Delay Time(IRFC1min),Least Significant Byte		00
SDRAM Minimum Refresh Recovery Delay Time(RFC2min),Most Significant Byte 861 SDRAM Minimum Refresh Recovery Delay Time(RFCsb),Least Significant Byte 862 SDRAM Minimum Refresh Recovery Delay Time(RFCsbmin),Most Significant Byte 863-890 RSVD,must be coded as 0x00 891 Advanced Memory Overclocking Features 892 System CMD Rate Mode 893 Vendor Personality Byte - RSVD 894 Oyclical Redundancy Code (CRC) for Base Configura tion Section, Most Significant Byte(for bytes 832-893) 895 Oyclical Redundancy Code (CRC) for Base Configura tion Section, Most Significant Byte(for bytes 832-893)	858	SDRAM Minimum Refresh Recovery Delay Time(IRFC1min) Most Significant Byte		00
SDRAM Minimum Refresh Recovery Delay Time(RFCsb),Least Significant Byte 862 SDRAM Minimum Refresh Recovery Delay Time(RFCsbmin),Most Significant Byte 863-850 RSVD,must be coded as 0x:00 861 Advanced Memory Overclocking Features 892 System CMD Rate Mode 893 Vendor Personality Byte - RSVD 894 Oyclical Redundancy Code (CRC) for Base Configura tion Section, Least Significant Byte(for bytes 832–893) 895 Oyclical Redundancy Code (CRC) for Base Configura tion Section, Most Significant Byte(for bytes 832–893) 896 Oyclical Redundancy Code (CRC) for Base Configura tion Section, Most Significant Byte(for bytes 832–893)	859	SDRAM Minimum Refresh Recovery Delay Time(RFC2min),Least Significant Byte		00
SDRAM Minimum Refresh Recovery Delay Time(RFCsbmin),Most Significant Byte 00	860	SDRAM Minimum Refresh Recovery Delay Time(RFC2min),Most Significant Byte		00
863-890 RSVD_must be coded as 0x00 00 891 Advanced Memory Overclocking Features 00 892 System CMD Rate Mode 00 893 Vendor Personality Byte - RSVD 00 894 Cyclical Redundancy Code (CRC) for Base Configura tion Section, Least Significant Byte(for bytes 832-893) 00 895 Cyclical Redundancy Code (CRC) for Base Configura tion Section, Most Significant Byte(for bytes 832-893) 00	861	SDRAM Minimum Refresh Recovery Delay Time(RFCsb).Least Significant Bytes		00
891 Advanced Memory Overclocking Features 00 892 System CMD Rate Mode 00 893 Vendor Personality Byte - RSVD 00 894 Cyclical Redundancy Code (CRC) for Base Configuration Section, Least Significant Byte/for bytes 832–893) 00 895 Cyclical Redundancy Code (CRC) for Base Configuration Section, Most Significant Byte/for bytes 832–893) 00	862	SDRAM Minimum Refresh Recovery Delay Time(RFCsbmin),Most Signiseent Byte		00
892 System CMD Rate Mode 893 Vendor Personality Byte - RSVD 894 Cyclical Redundancy Code (CRC) for Base Configuration Section, Least Significant Byte(for bytes 832–893) 895 Cyclical Redundancy Code (CRC) for Base Configuration Section, Most Significant Byte(for bytes 832–893) 896 Oyclical Redundancy Code (CRC) for Base Configuration Section, Most Significant Byte(for bytes 832–893)	863-890	RSVD,must be coded as 0x00		00
893 Vendor Personality Byte - RSVD 00 894 Cyclical Redundancy Code (CRC) for Base Configuration Section, Least Significant Byte(for bytes 832–893) 00 895 Cyclical Redundancy Code (CRC) for Base Configuration Section, Most Significant Byte(for bytes 832–893) 00	891	Advanced Memory Overclocking Features		00
894 Cyclical Redundancy Code (CRC) for Base Configura tion Section, Least Significant Byte(for bytes 832–893) 895 Cyclical Redundancy Code (CRC) for Base Configura tion Section, Most Significant Byte(for bytes 832–893)	892	System CMD Rate Mode		00
895 Cyclical Redundancy Code (CRC) for Base Configuration Section, Most Significant Byte(for bytes 832–893)	893	Vendor Personality Byte - RSVD	·	00
	894	Cyclical Redundancy Code (CRC) for Base Configura tion Section, Least Significant Byte(for bytes 832-893)		00
896-1023 User Settings 00	895	Oyclical Redundancy Code (CRC) for Base Configura tion Section, Most Significant Byte(for bytes 832-893)		00
	896-1023	User Settings		00

Note:

- 1. Byte 194-201 -- By SPD Hub & PMIC Vendor & Revision
- 1.1 Byte 194-201 By Gr B_RIBS & Filip & Fili

- 3. Byte 515 -- Module manufacturing date by year (YY). (Decimal)
- 4. Byte 516 -- Module manufacturing date by week (WW). (Decimal)
- 5. Bytes 517-520 -- Module Serial Number. (Decimal)
 6. Bytes 521-550 -- Module Part Number. (ASCII format, unused digits are coded as ASCII blanks (0x20).
 7. Bytes 552-553 -- DRAM Manufacturer ID Code by JEDEC definition. SAMSUNG :[(0x80) ,(0xCE)]
- 8. Bytes 555~639 -- These bytes are undefined and can be used own purpose