

262Pin DDR5 5600 1.1V SO-DIMM 16GB Based on 2048Mx8 AQD-SD5V16GN56-SB

Advantech

AQD-SD5V16GN56-SB Datasheet

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Description

AQD-SD5V16GN56-SB is DDR5-5600(CL46)-45-45 SDRAM memory module. The SPD is programmed to JEDEC standard latency 5600Mbps timing of 46-45-45 at 1.1V. The module is composed of 16Gb CMOS DDR5 SDRAMs in FBGA package and one 8Kbit SPD Hub in 8pin TDFN package on a 262pin glass–epoxy printed circuit board.

The module is a Dual In-line Memory Module and intended for mounting onto 262 pins edge connector sockets. Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features

- RoHS compliant products.
- JEDEC standard 1.1V(1.067V~1.166V) Power supply
- VDDQ= 1.1V(1.067V~1.166V)
- VPP = 1.8V(+0.108V / -0.054V)
- Data transfer rates: PC5-5600
- Programmable CAS Latency: 22,26,28,30,32,36,40,42,46
- 16 bit pre-fetch
- Burst Length (BL) switch on-the-fly BL16 or BC8
- Bi-directional Differential Data-Strobe
- On Die Termination, Nominal, Park
- Serial presence detect hub (SPD Hub) with
 Integrated Temperature sensor
- Asynchronous reset
- PCB edge connector treated with 30u" Gold-Plating



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Pin Name	Description	Pin Name	Description
CA0_A - CA12_A CA0_B - CA12_B	SDRAM Command/Address bus	HSCL	Side Band bus clock
CS0_A_n - CS1_A_n CS0_B_n - CS1_B_n	SDRAM Chip Select	HSDA	Side Band bus data
DQ0_A - DQ31_A DQ0_B - DQ31_B	DIMM memory data bus	HSA	Side Band bus address
CB0_A - CB3_A CB0_B - CB3_B	DIMM ECC check bits	ALERT_n	SDRAM ALERT_n
DQS0_A_t - DQS4_A_t DQS0_B_t - DQS4_B_t	SDRAM data strobes (positive line of differential pair)	RESET_n	Set DRAMs to a Known State
DQS0_A_c - DQS4_A_c DQS0_B_c - DQS4_B_c	SDRAM data strobes (negative line of differential pair)	VIN_BULK	5 V power input supply
DM0_A_n - DM3_A_n DM0_B_n - DM3_B_n	SDRAM data masks	VSS	Power supply return (ground)
CK0_A_t, CK1_A_t CK0_B_t, CK1_B_t	SDRAM clocks (positive line of differential pair)	PWR_GOOD	Power good indicator
CK0_A_c, CK1_A_c CK0_B_c, CK1_B_c	SDRAM clocks (negative line of differential pair)	PWR_EN	PMIC Enable
		RFU	Reserved for future use

DDR5 SO-DIMM has 2 channels (channel-A and channel-B) of signal bus.

The signals with suffix: _A (e.g. DQ0_A) are for channel-A, and the signals with suffix: _B (e.g. DQ0_B) are for channel-B



Dimensions (Unit: millimeter)



Note:1. Tolerances on all dimensions +/-0.15mm unless otherwise specified.



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Pin Assignments

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VIN_BULK	89	VSS	175	CB3_B	2	HSA	90	VSS	176	CB2_B
3	VIN_BULK	91	DQ30_A	177	VSS	4	HSCL	92	DQ31_A	178	VSS
5	RFU	93	VSS	179	DQ0_B	6	HSDA	94	VSS	180	DQ1_B
7	PWR_GOOD	95	CB0_A	181	VSS	8	PWR_EN	96	CB1_A	182	VSS
9	VSS	97	VSS	183	DQ2_B	10	VSS	98	VSS	184	DQ3_B
11	DQ0_A	99	CB2_A	185	VSS	12	DQ1_A	100	DQS4_A_c	186	VSS
13	VSS	101	VSS	187	DM0_B_n	14	VSS	102	DQS4_A_t	188	DQS0_B_c
15	DQ2_A	103	CB3_A	189	VSS	16	DQ3_A	104	VSS	190	DQS0_B_t
17	VSS	105	VSS	191	DQ4_B	18	VSS	106	CS0_A_n	192	VSS
19	DM0_A_n	107	CA0_A	193	VSS	20	DQS0_A_c	108	ALERT_n	194	DQ5_B
21	VSS	109	CA1_A	195	DQ6_B	22	DQS0_A_t	110	CS1_A_n	196	VSS
23	DQ4_A	111	VSS	197	VSS	24	VSS	112	VSS	198	DQ7_B
25	VSS	113	CA2_A	199	DQ8_B	26	DQ5_A	114	CA3_A	200	VSS
27	DQ6_A	115	CA4_A	201	VSS	28	VSS	116	CA5_A	202	DQ9_B
29	VSS	117	VSS	203	DQ10_B	30	DQ7_A	118	VSS	204	VSS
31	DQ8_A	119	CA6_A	205	VSS	32	VSS	120	CA7_A	206	DQ11_B
33	VSS	121	CA8_A	207	DQS1_B_c	34	DQ09_A	122	CA9_A	208	VSS
35	DQ10_A	123	VSS	209	DQS1_B_t	36	VSS	124	VSS	210	DM1_B_n
37	VSS	125	CA10_A	211	VSS	38	DQ11_A	126	CA11_A	212	VSS
39	DQS1_A_c	KEY		213	DQ12_B	40	VSS	KEY		214	DQ13_B
41	DQS1_A_t	127	CA12_A	215	VSS	42	DM1_A_n	128	RFU	216	VSS
43	VSS	129	VSS	217	DQ14_B	44	VSS	130	VSS	218	DQ15_B
45	DQ12_A	131	CK0_A_t	219	VSS	46	DQ13_A	132	CK1_A_t	220	VSS
47	VSS	133	CK0_A_c	221	DQ16_B	48	VSS	134	CK1_A_c	222	DQ17_B
49	DQ14_A	135	VSS	223	VSS	50	DQ15_A	136	VSS	224	VSS
51	VSS	137	CK0_B_t	225	DQ18_B	52	VSS	138	CK1_B_t	226	DQ19_B
53	DQ16_A	139	CK0_B_c	227	VSS	54	DQ17_A	140	CK1_B_c	228	VSS
55	VSS	141	VSS	229	DM2_B_n	56	VSS	142	VSS	230	DQS2_B_c
57	DQ18_A	143	RFU	231	VSS	58	DQ19_A	144	CA12_B	232	DQS2_B_t
59	VSS	145	CA11_B	233	DQ20_B	60	VSS	146	CA10_B	234	VSS
61	DM2_A_n	147	VSS	235	VSS	62	DQS2_A_c	148	VSS	236	DQ21_B
63	VSS	149	CA9_B	237	DQ22_B	64	DQS2_A_t	150	CA8_B	238	VSS
65	DQ20_A	151	CA7_B	239	VSS	66	VSS	152	CA6_B	240	DQ23_B
67	VSS	153	VSS	241	DQ24_B	68	DQ21_A	154	VSS	242	VSS
69	DQ22_A	155	CA5_B	243	VSS	70	VSS	156	CA4_B	244	DQ25_B
71	VSS	157	CA3_B	245	DQ26_B	72	DQ23_A	158	CA2_B	246	VSS
73	DQ24_A	159	VSS	247	VSS	74	VSS	160	VSS	248	DQ27_B
75	VSS	161	CS0_B_n	249	DQS3_B_c	76	DQ25_A	162	CA1_B	250	VSS
77	DQ26_A	163	RESET_n	251	DQS3_B_t	78	VSS	164	CA0_B	252	DM3_B_n
79	VSS	165	CS1_B_n	253	VSS	80	DQ27_A	166	VSS	254	VSS
81	DQS3_A_c	167	VSS	255	DQ28_B	82	VSS	168	CB0_B	256	DQ29_B
83	DQS3_A_t	169	DQS4_B_c	257	VSS	84	DM3_A_n	170	VSS	258	VSS
85	VSS	171	DQS4_B_t	259	DQ30_B	86	VSS	172	CB1_B	260	DQ31_B
87	DQ28_A	173	VSS	261	VSS	88	DQ29_A	174	VSS	262	VSS



Function Block Diagram

1Rank, x8 DDR5 SDRAMs

Channel A



Channel B





Note : ZQ resistors are $240\Omega \pm 1\%$.

HSCL

HSDA

HSA

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Operating Temperature Condition

	Parameter	Symbol	Rating	Unit	Note
Operating [•]	Temperature	TOPER	0 to 85	°C	1,2
Note:	Operating Temperature is the case surface temperature on the center/temeasurement conditions, please refer to JESD51-2 standard.	op side of th	ne DRAM. F	or the	

Absolute Maximum DC Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on VDD relative to Vss	VDD	-0.3 ~ 1.4	V	1
Voltage on VDDQ pin relative to Vss	VDDQ	-0.3 ~ 1.4	V	1
Voltage on any pin relative to Vss	VIN, VOUT	-0.3 ~ 1.4	V	1
Storage temperature	Tstg	-55~+100	°C	1,2

Note: 1. Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

AC & DC Operating Conditions

Recommended DC operating conditions

Deremeter	Symbol	Voltago		Rating		Unit	Notoo
Falameter	Symbol	vonage	Min	Тур.	Мах	Unit	Notes
Host Supply Voltage	VIN_BULK	12.0	4.25	5.0	5.5	V	
PMIC Output Supply Voltage	VDD	1.1	1.067	1.1	1.166	V	1,2,3
PMIC Output Supply Voltage	VDDQ	1.1	1.067	1.1	1.166	V	1,2,3
PMIC Output Supply Voltage	VPP	1.8	1.746	1.8	1,908	V	3
AC Input Logic High	VIH(AC)	TBD	-	-	-	mV	
AC Input Logic Low	VIL(AC)	TBD	-	-	-	mV	
DC Input Logic High	VIH(DC)	TBD	-	-	-	mV	
DC Input Logic Low	VIL(DC)	TBD	-	-	-	mV	

Note: (1) VDD must be within 66mv of VDDQ

(2) AC parameters are measured with VDD and VDDQ tied together.

(3) This includes all voltage noise from DC to 2 MHz at the DRAM package ball.



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IDD Specification parameters Definition - 16GB

Symbol	Condition	16GB	Unit
IDD0	One bank ACTIVATE-PRECHARGE current	TBD	mA
IDD0F	Operating Four Bank Active-Precharge Current	TBD	mA
IDD2N	Precharge Standby Current	TBD	mA
IDD2P	Precharge Power-Down Current	TBD	mA
IDD3N	Active standby current	TBD	mA
IDD3P	Active Power-Down Current	TBD	mA
IDD4R	Burst Read Current	TBD	mA
IDD4W	Burst write current	TBD	mA
IDD5B	Burst Refresh Current (1x REF)	TBD	mA
IDD5C	Burst Refresh Current (Same Bank Refresh Mode)	TBD	mA
IDD6N	Self refresh current: Normal temperature range (0–85°C)	TBD	mA
IDD7	Bank interleave read current	TBD	mA
IDD8	Maximum power-down current	TBD	mA



Timing Param	eters & Sp	ecificatio	ons						
Devenuetor	Cumhal	DDR5	-4800	DDR5-	-5600	DDR	DDR5-6400		Notes
Parameter	Symbol	Min	Мах	Min	Мах	Min	Мах	Unit	Notes
	1	1	Clock	Timing		1	1	1	
Clock period average	tCK (AVG)	0.416	<0.454	0.357	<0.384	0.312	<0.333	ns	1
	•		Command and	Address Timing	9				
Read to Read command delay for same bank group	tCCD_L	max(8nCK, 5ns)	_	max(8nCK, 5ns)	_	max(8nCK, 5ns)	_	nCK,ns	8
Write to Write command delay for same bank groupp	tCCD_L_WR	max(32nCK, 20ns)	_	max(32nCK, 20ns)	-	max(32nCK, 20ns)	_	nCK,ns	8
Write to Write command delay for same bank group, second write not RMW	tCCD_L_WR2	max(16nCK, 10ns)	_	max(16nCK, 10ns)	_	max(16nCK, 10ns)	_	nCK,ns	8
Read to Write command delay for same bank group	tCCD_L_RTW		CL - CV	/L + RBL/2 + 2tC + (tRPST - 0.5t0	:K - (Read DQS CK) + tWPRE	S offset)		nCK,ns	3,5,6,8
Write to Read command delay for same bank group	tCCD_L_WTR		C	WL + WBL/2 + M	ax(16nCK,10n	5)		nCK,ns	4,6,8
Read to Read command delay for different bank group	tCCD_S	8	_	8	_	8	_	nCK	8
Write to Write command delay for different bank group	tCCD_S_WR	8	_	8	_	8	_	nCK	8
Read to Write command delay for different bank group	tCCD_S_RTW	CL - CV	NL + RBL/2 + 2	tCK - (Read DQS	S offset) + (tRP	ST - 0.5tCK) + t	WPRE	nCK,ns	3,5,6,8
Write to Read command delay for different bank group	tCCD_S_WTR		С	WL + WBL/2 + M	lax(4nCK,2.5ns	\$)		nCK,ns	4,6,8
Write to Read with Auto Precharge command delay for same bank	tCCD_WTRA			CWL + WBL/2 -	+ tWR - tRTP			nCK,ns	2,4,6,8



		DDR5	-4800	DDR5-5600		DDR5-6400			
Parameter	Symbol	Min	Мах	Min	Max	Min	Мах	Unit	Notes
Activate to Activate command delay to same bank group for 1KB page size	tRRD_L(1K)	max(8nCK, 5ns)	_	max(8nCK, 5ns)	_	max(8nCK, 5ns)	_	nCK,ns	8
Activate to Activate command delay to same bank group for 2KB page size	tRRD_L(2K)	max(8nCK, 5ns)	_	max(8nCK, 5ns)	_	max(8nCK, 5ns)	_	nCK,ns	8
Activate to Activate command delay to different bank group for 1KB page size	tRRD_S(1K)	8	_	8	_	8	_	nCK	8
Activate to Activate command delay to different bank group for 2KB page size	tRRD_S(2K)	8	-	8	-	8	-	nCK	8
Four activate window for 1KB page size	tFAW (1K)	Max(32nCK, 13.333ns)	_	Max(32nCK, 11.428ns)	_	Max(32nCK, 10.000ns)	_	nCK,ns	
Four activate window for 2KB page size	tFAW (2K)	Max(40nCK, 16.666ns)	_	Max(40nCK, 14.285ns)	_	Max(40nCK, 12.500ns)	_	nCK,ns	
Read to Precharge command delay	tRTP	Max(12nCK, 7.5ns)	_	Max(12nCK, 7.5ns)	_	Max(12nCK, 7.5ns)	_	nCK,ns	8
Precharge to Precharge command delay	tPPD	2	_	2	_	2	_	nCK	7,8
Write recovery time	tWR	30	_	30	_	30	_	ns	8



Notes:

- 1. tCK(avg)min listed for reference only, refer to the Speed Bins and Operations section which lists all valid tCK(avg) values.
- 2. tCCD_WTRA(min) shall always be greater than or equal to CWL + WBL/2 + tWR(min) tRTP(min), and when using the appropriate rounding algorithms,

nCCD_WTRA(min) shall always be greater than or equal to CWL + WBL/2 + nWR(min) - nRTP(min).

- 3. RBL: Read burst length associated with Read command
 - RBL = 32 (36 w/ RCRC on) for fixed BL32 and BL32 in BL32 OTF mode
 - RBL = 16 (18 w/ RCRC on) for fixed BL16 and BL16 in BL32 OTF mode
 - RBL = 16 (18 w/ RCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode
- 4. WBL: Write burst length associated with Write command
 - WBL = 32 (36 w/ WCRC on) for fixed BL32 and BL32 in BL32 OTF mode
 - WBL = 16 (18 w/ WCRC on) for fixed BL16 and BL16 in BL32 OTF mode
 - WBL = 16 (18 w/ WCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode
- 5.5 The following is considered for tRTW equation
 - 1tCK needs to be added due to tDQS2CK
 - Read DQS offset timing can pull in the tRTW timing
 - 1tCK needs to be added when 1.5tCK postamble
- 6. CWL=CL-2
- 7. tPPD applies to any combination of precharge commands (PREab, PREsb, PREpb). tPPD also applies to any combination of precharge commands to a different die in a

3DS DDR5 SDRAM.

8. This parameter only specifies minimum values (there is no maximum value). The maximum value cells have been merged in

the table to improve legibility.



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Byte	Function Described	Fund	tion	HEX Val
0	Number of Butes in SPD Device	SPD Total:	1024Bytes	,
-				
1	SPD Revision for Base Configuration Parameters	Versio	xn 1.1	
2	Key Byte / Host Bus Command Protocol Type	DUKS S	ILIKAM	
4	Ret SDRAM Desclis and Backage	000	16/25	
-	Hist SUPAN Definitive and Package	Monolithic SDRAM Row: 16	Colume : 10	
6	Hist Survey Addressing	NOW . TO	e countri tu	
7	miss Survey in Company Reads Revealed Company Street Company Street Survey Street Survey Street Survey Street Stre	R back orouge/4 ba	o oko peribank omun	
8	In the Gorden Date Catological Destina Catologica	o ben groupare de	nika per bienk group	
9	Second SDRAM Addression			
10	Secondary SRFAM (UV) with			
11	Second SDRAM Bank Groups & Banks Per Bank Group			
		One repair element per		
12	SDRAM BL32 & Post Package Repair	bank group	Burst length 32 supported	
13	SDRAM Duty Cycle Adjuster & Partial Array Self Refresh	Device supports DCA for	4-phase internal clock(s)	
14	SDRAM Fault Handling	Writeback suppress	ion control in MR9	
15	Reserved	must be cod	led as 0x00	(
16	SDRAM Nominal Voltage, VDD	Operable:1.1V	Endurant:1.1V	(
17	SDRAM Nominal Voltage, VDDQ	Operable:1.1V	Endurant:1.1V	0
18	SDRAM Nominal Voltage, VPP	Operable:1.8V	Endurant:1.8V	
19	SDRAM Timing	Standard core timir	ngs per JESD79-5	0
20	SDRAM Minimum Cycle Time (ICKAVGmin), Least Significant Byte			
21	SDRAM Minimum Cycle Time (tCKAVGmin), Most Significant Byte	357	ps	(
22	SDRAM Maximum Cycle Time (tCKAVGmax), Least Significant Byte			F
23	SDRAM Maximum Cycle Time (ICKAVGmax), Most Significant Byte	1010	ps	(
24	SDRAM CAS Latencies Supported:First Byte	CL22,26,	28,30,32	7
25	SDRAM CAS Latencies Supported Second Byte	CL,36,40,	42,46,50	A
26	SDRAM CAS Latencies Supported:Third Byte			(
27	SDRAM CAS Latencies Supported Fourth Byte			(
28	SDRAM CAS Latencies Supported:Fith Byte			(
29	Reserved	must be cod	ied as 0x00	(
30	SDRAM Minimum CAS Latency Time (tAAmin), Least Significant Byte	18000		8
31	SDRAM Minimum CAS Latency Time (tAAmin), Most Significant Byte	10000	ps	3
32	SDRAM Minimum RAS to CAS Delay Time (IRCDmin), Least Significant Byte	18000		1
33	SDRAM Minimum RAS to CAS Delay Time (RCDmin), Most Significant Byte	10000	pa -	3
34	SDRAM Minimum Row Precharge Delay Time (tRPmin), Least Significant Byte	18000	06	· · · ·
35	SDRAM Minimum Row Precharge Delay Time (tRPmin), Most Significant Byte	10000	pa -	3
36	SDRAM Minimum Active to Precharge Delay Time (IRASmin), Least Significant Nibble	32000	05	(
37	SDRAM Minimum Active to Precharge Delay Time (IRASmin), Most Significant Byte			7
38	SDRAM Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Nibble	48000	05	
39	SDRAM Minimum Active to Active/Refresh Delay Time (IRCmin), Most Significant Nibble		-	В
40	SDRAM Minimum Write Recovery Time (WRmin), Least Significant Nibble	30000	ps	
41	SURVAM Minimum Write Recovery Time (WRmin), Mest Significant Nibble			
42	SDRVM Minimum Retrosh Recovery Delay Time (RFC1 min, IRFC1 sir min).Least Significant Byte	295	ns	
43	SDRAM Minimum Refresh Recovery Delay Time (IRFC1 min, IRFC1 sir min). Most Significant Byte			r (
44	SLRVan Minimum Korrosh Recovery Delay Time (RFC27), RFC2 sir minjLeast Significant Byte	160	ns	
45	SURVAM Minimum Renesh Recovery Delay Time (RRC2min, RRC2 sir min),Most Significant Byte			
46	SDRAM Minimum Retrish Recovery Delay Time (RRFCsbmin, RRFCsb sir min),Least Significant Byte	130	ns	
47	SURVive minimum rearrish Recovery Delay Time (RH-LSOMIN, RH-LSO SI mini, RH-LSO SI			
48	SURVair Minimum Remean Recovery belay Time, SDS Different Logical Rank(RFCC) or miniLeast significant Byte	monolithic	SDRAMs	
49	SURVive minimum Remain Recovery Delay Time, sub-Dimensi Logical Kankipe-C1 di mini/Most Significant Byte			
50	Server memory rearran reactivery being imme, des uninterni Lagical Paragrer 22 offentingLess significant 89/0 EPENM Missioner Belance Beaurage 1 200 Different Lagical Paragrer 22 offentingLess significant 89/0	monolithic	SDRAMs	
62	Survey minimum Average Recovery Delay Time, 325 Universit Logical RankprvC2 of mini,M051 Significant Byte DRAM Historium Reference Recovery Delay Time, 305 Different Logical RankprvC2 of the International Rank			
52	Sections memory reveals nectority being time, sub cinema Logice Reingroups of minipless significant Byte DRAM Minipum Release Recovery Delay Time, 305 Different Logical Relia(BEC): A direction Minipuest Builty	monolithic	SDRAMs	
54	DEPONDENTIAL DEPONDENT PRESENT PRESENT DE LA DESTRUCTURA DE LA DEPONDENTIAL DE LA DEPONDENTIAL DE LA DESTRUCTURA DE LA D	+		
54	DEPONDE PONTIART I MINISTRATING DE			
56	SRRAM Refresh Management Birth Nulls Second SRRAM			
67	SERVICE Refresh Management Second SUBAM			
	and a constrained constrained on the second s	1		L
58	SDRAM Adaptive Refresh Management, First SDRAM, First Byte Level A			r (
58	SDRAM Adaptive Refresh Management, First SDRAM, First Byte,Level A SDRAM Adaptive Refresh Management, First SDRAM, Second Byte Level A			

60 SDRAM Adaptive Refresh Management, Second SDRAM, First Byte,Level A



61	SDRAM Adaptive Refresh Management, Second SDRAM, Second Byte,Level A		00
62	SDRAM Adaptive Refresh Management, First SDRAM, First Byte,Level B		00
63	SDRAM Adaptive Refresh Management, First SDRAM, Second Byte,Level B		00
64	SDRAM Adaptive Refresh Management, Second SDRAM, First Byte,Level B		00
65	SDRAM Adaptive Refresh Management, Second SDRAM, Second Byte Level B		00
66	SDRAM Adaptive Refresh Management, First SDRAM, First Byte Level C		00
67	SDRAM Adaptive Refresh Management, First SDRAM, Second Byte Level C		00
68	SDRAM Adaptive Retresh Management Second SDRAM First Byte Level C		00
60	Contrain Assignment Assignment Section Software, mar Synchronia Contrained and Co		00
70	COPONE response rearrain memory and common concerned and any second and any concerned any concerne		88
70	Software Minimum Active to Active Command Delay Time, Same Bank Goop, Arch Ching Datast significant byte	5000 ps	12
	SURVAN Minimum Active to Active Command Delay Time, Same Bank Group, GPGD Limin, Most Signin Cant Byte	a -CK	10
72	SDRAM Minimum Active to Active Command Delay Time, Same Bank Group,(RRD Lmin),Lower Clock Limit	8 10 K	00
73	SDRAM Minimum CAS in to CAS in Command Delay Time, Same Bank Group,(tCCD Lmin),Least Significant Byte	5000 ps	88
74	SDRAM Minimum CAS in to CAS in Command Delay Time, Same Bank Group,(tCCD Lmin),Most Significant Byte	-	13
75	SDRAM Minimum CAS in to CAS in Command Delay Time, Same Bank Group,(tCCD Lmin),Lower Clock Limit	8 nCK	08
76	SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (tCCD L WRmin),Least Significant Byte	20000 ps	20
77	SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (tCCD L WRmin),Most Significant Byte		4E
78	SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (tCCD L. WRmin),Lower Clock Limit	32 nCK	20
79	SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (tCCD L. WR2min),Least Significant Byte	10000 cs	10
80	SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (ICCD L WR2min),Most Significant Byte	10000 pa	27
81	SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (tCCD L. WR2min),Lower Clock Limit	16 nCK	10
82	SDRAM Minimum Four Activate Window (tFAWmin).Least Significant Byte	11428	A4
83	SDRAM Minimum Four Activate Window (IFAWmin),Most Significant Byte	11420 ps	2C
84	SDRAM Minimum Four Activate Window (#FAWmin),Lower Clock Limit	32 nCK	20
85	SDRAM Write to Read Command Delay for Same Bank Group (tCCD L WTR) Least Significant Byte		10
86	SDRAM Write to Read Command Delay for Same Bank Group (ICCD L WTR), Most Significant Byte	10000 ps	27
87	SDRAM Write to Read Command Delay for Same Bank Group (tCCD L WTR)Lower Clock Limit	16 nCK	10
88	SDRAM Write to Read Command Delay for Different Bank Group (ICCD S WTR) Least Significant Byte		C4
89	SDRAM White in Read Command Data for Different Bank Group (CCD 5 WTR) Meet Stinding they	2500 ps	09
90	Control white to head command being to of many being local of the many factor of the many factor of the second sec	4 pCK	
	Solven where there command being for the method solution of the control of the co	4100	40
91	School Association of Pachage Command Datey (KTP, KTP, Sing, Cass Significant Syst	7500 ps	+0
00	COOAL Dead is Dealering Command Delay (2010) 1010 and Clark Clark Cont		10
92	SDRAM Read to Precharge Command Delay (RTP, RTP sir), Most Significant Byte	10 - 2 K	1D
92 93	SDRAM Read to Precharge Command Delay (RTP, RTP sir), Most Significant Byte SDRAM Read to Precharge Command Delay (RTP, RTP sir), Lower Clock Limit	12 nCK	1D 0C
92 93 94-127	SDRAM Read to Precharge Command Delay (RTP, IRTP sir), Most Significant Byte SDRAM Read to Precharge Command Delay (RTP, IRTP sir), Lower Clock Limit Reserved, Base Configuration Section	12 nCK Must be coded as 0x00	1D 0C 00
92 93 94-127 128-191	SDRAM Read to Precharge Command Delay (RTP, IRTP sir), Most Significant Byte SDRAM Read to Precharge Command Delay (RTP, IRTP sir), Lower Clock Limit Reserved, Base Configuration Section Reserved for future use	12 nCK Must be coded as 0x00 Reserved for future use	1D 0C 00
92 93 94-127 128-191 192	SDRAM Read to Precharge Command Delay (RTP, RTP sir), Most Significant Byte SDRAM Read to Precharge Command Delay (RTP, tRTP sir), Lower Clock Limit Reserved, Base Configuration Section Reserved for future use SPD Revision for Module Information	12 nCK Must be coded as 0x00 Reserved for future use Version 1.0	1D 0C 00 00
92 93 94-127 128-191 192 193	SDRAM Read to Precharge Command Delay (RTP, RTP sir), Most Significant Byte SDRAM Read to Precharge Command Delay (RTP, tRTP sir), Lower Clock Limit Reserved, Base Configuration Section Reserved for future use SPD Revision for Module Information Hashing Sequence	12 nCK Must be coded as 0x00 Reserved for future use Version 1.0 No authentication	1D 0C 00 10 00
92 93 94-127 128-191 192 193 194	SDRAM Read to Precharge Command Delay (RTP, RTP sin), Most Significant Byte SDRAM Read to Precharge Command Delay (RTP, tRTP sin), Lower Clock Limit Reserved of future use SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte	12 nCK Must be coded as 0x00 Reserved for future use Version 1.0 No authentication	1D 0C 00 10 00
92 93 94-127 128-191 192 193 194 195	SDRAM Read to Precharge Command Delay (RTP, RTP sir), Most Significant Byte SDRAM Read to Precharge Command Delay (RTP, IRTP sir), Lower Clock Limit Reserved, Base Configuration Section Reserved for future use SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Manufacturer ID Code, Second Byte	12 nCK Must be coded as 0x00 Reserved for future use Version 1.0 No authentication	1D 0C 00 10 00
92 93 94-127 128-191 192 193 194 195 196	SDRAM Read to Precharge Command Delay (RTP, RTP sir), Most Significant Byte SDRAM Read to Precharge Command Delay (RTP, tRTP sir), Lower Clock Limit Reserved. The Section Reserved for future use SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Manufacturer ID Code, Second Byte SPD Device Type	12 nCK Must be coded as 0x00 Reserved for future use Version 1.0 No authentication	1D 0C 00 10 00
92 93 94-127 128-191 192 193 194 195 196 197	SIRAM Read to Precharge Command Delay (RTP, RTP sir), Most Significant Byte SDRAM Read to Precharge Command Delay (RTP, tRTP sir), Lower Clock Limit Reserved asse Configuration Section Reserved asse Configuration Section SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Manufacturer ID Code, Second Byte SPD Device Type SPD Device Revision Number	12 nCK Must be coded as 0x00 Reserved for future use Version 1.0 No authentication	1D 0C 00 10 00
92 93 94-127 128-191 192 193 194 195 196 197 198	SIRAM Read to Precharge Command Delay (RTP, RTP sin, Most Significant Byte SDRAM Read to Precharge Command Delay (RTP, tRTP sin, Lower Clock Limit Reserved for future use SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Device Type SPD Device Revision Number PMIC 0 Manufacturer ID Code, First Byte	12 nCK Must be coded as 0x00 Reserved for future use Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision	1D 0C 00 10 00
92 93 94-127 128-191 192 193 194 195 196 197 198	SIRAM Read to Precharge Command Delay (RTP, RTP sin, Most Significant Byte SDRAM Read to Precharge Command Delay (RTP, tRTP sin, Lower Clock Limit Reserved , Base Configuration Section Reserved for future use SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Device Revision Number PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Manufacturer ID Code, Second Byte SPD Manufacturer ID Code, First Byte	12 nCK Must be coded as 0x00 Reserved for future use Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision "Note: 1	1D 0C 00 10 00
92 93 94-127 128-191 192 193 194 195 196 197 198 199	SDRAM Read to Precharge Command Delay (RTP, RTP sir), Most Significant Byte SDRAM Read to Precharge Command Delay (RTP, IRTP sir), Lower Clock Limit Reserved asso Configuration Section Reserved for future use SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Device Revision Number PMIC 0 Manufacturer ID Code, Second Byte PMIC 0 Manufacturer ID Code, Second Byte	12 nCK Must be coded as 0x00 Reserved for future use Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision "Note: 1	1D 0C 00 10 00
92 93 94-127 128-191 192 193 194 195 196 197 198 199 200	SDRAM Read to Precharge Command Delay (RTP, RTP sin, Most Significant Byte SDRAM Read to Precharge Command Delay (RTP, RTP sin, Lower Clock Limit Reserved. Base Configuration Section Reserved for future use SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Device Type SPD Device Revision Number PMIC 0 Manufacturer ID Code, Second Byte PMIC 0 Device Type	12 nCK Must be coded as 0x00 Reserved for future use Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision *Note: 1	1D 00 00 10 00
92 93 94-127 128-191 192 193 194 195 196 197 198 199 200 201	SIRAM Read to Precharge Command Delay (RTP, RTP sin, Most Significant Byte SDRAM Read to Precharge Command Delay (RTP, IRTP sin, Lower Clock Limit Reserved for future use Reserved fase Configuration Section Reserved fase Configuration Reserved for future use SPD Revision for Module Information Hashing Sequence SPD Revision for Module Information SPD Manufacturer ID Code, First Byte SPD Device Type PMIC 0 Manufacturer ID Code, Second Byte PMIC 0 Device Type PMIC 0 Revision Number PMIC 0 Revision Number	12 nCK Must be coded as 0x00 Reserved for future use Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision "Note: 1	1D 0C 00 10
92 93 94-127 128-191 192 193 194 195 196 197 198 199 200 201 201 202	SIRAM Read to Precharge Command Delay (RTP, RTP sin, Most Significant Byte SDRAM Read to Precharge Command Delay (RTP, tRTP sin, Lower Clock Limit Reserved for future use SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Device Type PMIC 0 Manufacturer ID Code, Second Byte PMIC 0 Manufacturer ID Code, Second Byte PMIC 0 Revision Number PMIC 0 Revision Number PMIC 0 Revision Number PMIC 1 Manufacturer ID Code, First Byte	12 nCK Must be coded as 0x00 Reserved for future use Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision "Note: 1	1D 0C 00 10 00
92 93 94-127 128-191 192 193 194 195 196 197 198 199 200 201 201 201 202 203	SDRAM Read to Precharge Command Delay (RTP, RTP sin, Most Significant Byte SDRAM Read to Precharge Command Delay (RTP, IRTP sin, Lower Clock Limit Reserved for future use SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Device Type SPD Device Revision Number PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Revision Number PMIC 1 Manufacturer ID Code, Second Byte PMIC 1 Manufacturer ID Code, Second Byt	12 nCK Must be coded as 0x00 Reserved for future use Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision "Note: 1	1D 000 000 100
92 93 94-127 128-191 192 193 194 195 196 197 198 199 200 201 201 202 202 203 204	SDRAM Read to Precharge Command Delay (RTP, RTP sin, Most Significant Byte SDRAM Read to Precharge Command Delay (RTP, RTP sin, Lower Clock Limit Reserved. Rese Configuration Section Reserved for future use SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Device Type SPD Device Type PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Nanufacturer ID Code, First Byte PMIC 0 Revision Number PMIC 10 Revision Number	12 nCK Must be coded as 0x00 Reserved for future use Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision "Note: 1	1D 00 00 10 00
92 93 94-127 128-191 192 193 194 195 196 197 198 199 200 201 202 203 204 205	SDRAM Read to Precharge Command Delay (RTP, RTP sin, Most Significant Byte SDRAM Read to Precharge Command Delay (RTP, RTP sin, Lower Clock Limit Reserved. Issae Configuration Section Reserved for future use SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Manufacturer ID Code, Second Byte SPD Device Revision Number PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Manufacturer ID Code, Second Byte PMIC 0 Revision Number PMIC 0 Revision Number PMIC 1 Manufacturer ID Code, First Byte PMIC 1 Manufacturer ID Code, Second Byte PMIC 1 Manufacturer ID Code, Second Byte	12 nCK Must be coded as 0x00 Reserved for future use Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision "Note: 1	1D 000 000 10 000 000 000 000 000 000 00
92 93 94-127 128-191 192 193 194 195 196 197 198 199 200 201 200 201 202 203 204 205 206	SDRAM Read to Precharge Command Delay (RTP, RTP sin, Most Significant Byte SDRAM Read to Precharge Command Delay (RTP, IRTP sin, Lower Clock Limit Reserved for future use Reserved for future use SPD Revision for Module Information Hashing Sequence SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Device Type PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Manufacturer ID Code, Second Byte PMIC 0 Manufacturer ID Code, Second Byte PMIC 0 Nanufacturer ID Code, Second Byte PMIC 0 Revision Number PMIC 0 Revision Number PMIC 1 Manufacturer ID Code, Second Byte PMIC 1 Revision Number	12 nCK Must be coded as 0x00 Reserved for future use Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision "Note: 1	1D 000 000 100 000 000 000 000 000 000 0
92 93 94-127 128-191 192 193 194 195 196 196 197 198 199 200 201 202 203 204 205 206 205 206	SDRAM Read to Precharge Command Delay (RTP, RTP sin, Most Significant Byte SDRAM Read to Precharge Command Delay (RTP, IRTP sin, Lower Clock Limit Reserved for future use SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Manufacturer ID Code, Second Byte SPD Device Type SPD Device Revision Number PMIC 0 Manufacturer ID Code, Second Byte PMIC 0 Device Type PMIC 0 Device Type PMIC 0 Revision Number PMIC 1 Manufacturer ID Code, Second Byte PMIC 1 Manufacturer ID Code, Second Byte PMIC 1 Manufacturer ID Code, Second Byte PMIC 1 Manufacturer ID Code, Rist Byte PMIC 1 Manufacturer ID Code, Rist Byte PMIC 1 Manufacturer ID Code, Second Byte	12 nCK Must be coded as 0x00 Reserved for future use Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision "Note: 1	1D 000 000 100 000 000 000 000 000 000 0
92 93 94-127 128-191 192 193 194 195 195 196 197 198 199 200 201 200 201 200 201 202 200 201 202 204 205 206 207 206	SDRAM Read to Precharge Command Delay (RTP, RTP sin, Most Significant Byte SDRAM Read to Precharge Command Delay (RTP, RTP sin, Lower Clock Limit Reserved, Base Configuration Section Reserved for future use SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Device Type SPD Device Type SPD Device Revision Number PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Revision Number PMIC 0 Revision Number PMIC 10 Revision Number PMIC 12 Revision Number	12 nCK Must be coded as 0x00 Reserved for future use Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision "Note: 1	1D 000 000 10 000 000 000 000 000 000 00
92 93 94-127 128-191 192 193 194 195 196 197 198 199 200 201 200 201 202 203 200 205 206 207 206 207 206	SDRAM Read to Precharge Command Delay (RTP, RTP sin, Most Significant Byte SDRAM Read to Precharge Command Delay (RTP, RTP sin, Lower Clock Limit Reserved. Base Configuration Section Reserved for future use SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Device Type SPD Device Type SPD Device Revision Number PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Nanufacturer ID Code, First Byte PMIC 0 Revision Number PMIC 0 Revision Number PMIC 1 Manufacturer ID Code, First Byte PMIC 1 Manufacturer ID Code, Second Byte PMIC 1 Device Type PMIC 1 Manufacturer ID Code, Second Byte PMIC 2 Device Type	12 nCK Must be coded as 0x00 Reserved for future use Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision "Note: 1	1D 000 000 10 000 000 000 000 000 000 00
92 93 94-127 128-191 192 193 194 195 196 197 198 199 200 201 202 203 204 205 206 206 207 208 209 206	SDRAM Read to Precharge Command Delay (RTP, RTP sin, Most Significant Byte SDRAM Read to Precharge Command Delay (RTP, IRTP sin, Lower Clock Limit Reserved. Issee Configuration Section Reserved for future use SPD Revision for Module Information Hashing Sequence SPD Revision To Code, First Byte SPD Manufacturer ID Code, First Byte SPD Device Type SPD Device Type PMIC 0 Manufacturer ID Code, Second Byte PMIC 0 Nanufacturer ID Code, First Byte PMIC 0 Nanufacturer ID Code, Second Byte PMIC 0 Revision Number PMIC 0 Revision Number PMIC 1 Manufacturer ID Code, First Byte PMIC 1 Manufacturer ID Code, First Byte PMIC 1 Manufacturer ID Code, Second Byte PMIC 1 Revision Number PMIC 1 Revision Number PMIC 2 Manufacturer ID Code, Second Byte PMIC 2 Manufacturer ID Code, Second Byte PMIC 2 Manufacturer ID Code, Second Byte PMIC 2 Revision Number PMIC 2 Revision Number PMIC 2 Revision Number PMIC 2 Revision Number PMIC 2 Revision Number	12 nCK Must be coded as 0x00 Reserved for future use Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision "Note: 1	1D 000 000 10 000 000 000 000 000 000 00
92 93 94-127 128-191 193 194 195 196 197 198 199 200 201 202 203 204 205 206 205 206 207 208 209 210 209 210	SDRAM Read to Precharge Command Delay (RTP, RTP sin, Most Significant Byte SDRAM Read to Precharge Command Delay (RTP, IRTP sin, Lower Clock Limit Reserved for future use SPD Revision for Module Information Hashing Sequence SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Device Type SPD Device Type PMIC 0 Manufacturer ID Code, Second Byte PMIC 0 Manufacturer ID Code, Second Byte PMIC 0 Nanufacturer ID Code, Second Byte PMIC 0 Nanufacturer ID Code, Second Byte PMIC 0 Manufacturer ID Code, Second Byte PMIC 0 Nanufacturer ID Code, Second Byte PMIC 1 Manufacturer ID Code, Second Byte PMIC 2 Revision Number PMIC 3 Revision Number PMIC 3 Revision Number PMIC 4 Revision Number PMIC 4 Revision Number PMIC 5 Revision Number	12 nCK Must be coded as 0x00 Reserved for future use Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision "Note: 1	1D 00 00 00 00 00 00 00 00 00 00 00 00 00
92 93 94-127 128-191 192 193 194 195 196 197 198 199 200 201 200 201 202 200 201 202 204 205 206 207 208 209 210 210 210	SDRAM Read to Precharge Command Delay (RTP, RTP sin, Most Significant Byte SDRAM Read to Precharge Command Delay (RTP, RTP sin, Lower Clock Limit Reserved. Base Configuration Section Reserved for future use SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Device Type SPD Device Type SPD Device Revision Number PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Nanufacturer ID Code, First Byte PMIC 1 Manufacturer ID Code, Second Byte PMIC 1 Manufacturer ID Code, First Byte PMIC 1 Manufacturer ID Code, First Byte PMIC 1 Manufacturer ID Code, Second Byte PMIC 1 Manufacturer ID Code, First Byte PMIC 2 Manufacturer ID Code, First Byte	12 nCK Must be coded as 0x00 Reserved for future use Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision "Note: 1	1D 000 000 10 000 000 000 000 000 000 00
92 93 94-127 128-191 192 193 194 195 196 197 198 199 200 201 202 203 204 205 206 207 208 209 209 209 209 209 200 201 201 202 203 204 205 206 207 208 209 209 210 211 211 211 212 211 212 211 212 212	SDRAM Read to Precharge Command Delay (RTP, RTP sin, Most Significant Byte SDRAM Read to Precharge Command Delay (RTP, RTP sin, Lower Clock Limit Reserved. Base Configuration Section Reserved for future use SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Device Type SPD Device Type SPD Device Revision Number PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Nanufacturer ID Code, First Byte PMIC 1 Manufacturer ID Code, Second Byte PMIC 1 Revision Number PMIC 2 Manufacturer ID Code, Second Byte PMIC 2 Revision Number PMIC 3 Revision Number PMIC 4 Revision Number PMIC 4 Revision Number PMIC 5 Revision Number PMIC 5 Revision Number PMIC 6 Revision Number PMIC 7 Revision Number PMIC 7 Revision Number PMIC 7 Revision Number PMIC 7 Revision Number PMIC 8 Revision Number PMIC 8 Revision Number PMIC 9 Revision Number PMIC	12 nCK Must be coded as 0x00 Reserved for future use Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision "Note: 1	1D 000 000 10 000 000 000 000 000 000 00
92 93 94-127 128-191 192 193 194 195 196 197 198 199 200 201 202 203 204 205 205 206 207 208 209 205 206 207 208 209 211 212 211 212	SDRAM Read to Precharge Command Delay (KTP, KTP sir), Most Significant Byte SDRAM Read to Precharge Command Delay (KTP, KTP sir), Lower Clock Limit Reserved. Sae Configuration Section Reserved for future use SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Manufacturer ID Code, Second Byte SPD Device Type PMIC 0 Manufacturer ID Code, Second Byte PMIC 0 Manufacturer ID Code, Second Byte PMIC 0 Manufacturer ID Code, Second Byte PMIC 1 Manufacturer ID Code, Second Byte PMIC 2 Revision Number PMIC 3 Revision Number PMIC 3 Revision Number PMIC 4 Revision Manufacturer ID Code, First Byte PMIC 2 Revision Manufacturer ID Code, Second Byte PMIC 2 Revision Number PMIC 3 Revision Number PMIC 4 Revision Manufacturer ID Code, Second Byte PMIC 2 Revision Manufacturer ID Cod	12 nCK Must be coded as 0x00 Reserved for future use Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision "Note: 1	1D 000 000 10 000 000 000 000 000 000 00
92 93 94-127 128-191 192 193 194 195 196 197 198 199 200 201 202 203 204 205 207 208 209 210 211 212 213 214	SDRAM Read to Precharge Command Delay (RTP, IRTP sin, Most Significant Byte SDRAM Read to Precharge Command Delay (RTP, IRTP sin, Lower Clock Limit Reserved, Base Configuration Section Reserved for future use SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Manufacturer ID Code, Second Byte SPD Device Type SPD Device Type PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Manufacturer ID Code, Rist Byte PMIC 0 Nanufacturer ID Code, Rist Byte PMIC 0 Revision Number PMIC 0 Revision Number PMIC 1 Manufacturer ID Code, Rist Byte PMIC 2 Manufacturer ID Code, Rist Byte PMIC 2 Manufacturer ID Code, Rist Byte PMIC 2 Device Type PMIC 3 Device Type PMIC 3 Device Type PMIC 4 Device Type	12 nCK Must be coded as 0x00 Reserved for future use Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision "Note: 1	1D 000 000 000 000 000 000 000 000 000 0
92 93 94-127 128-191 192 193 194 195 196 197 198 199 200 201 202 203 204 205 206 206 206 207 208 209 210 211 212 213 214 215	SIRAM Read to Precharge Command Delay (RTP, IRTP sin, Most Significant Byte SDRAM Read to Precharge Command Delay (RTP, IRTP sin, Lower Clock Limit Reserved, Base Configuration Section Reserved for future use SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Manufacturer ID Code, Second Byte SPD Device Type PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Nanufacturer ID Code, First Byte PMIC 1 Manufacturer ID Code, First Byte PMIC 2 Device Type PMIC 2 Manufacturer ID Code, First Byte PMIC 2 Manufacturer ID Code, First Byte PMIC 2 Revision Number PMIC 3 Revision Number PMIC 3 Revision Number PMIC 4 Revision Number PMIC 5 Revisio	12 nCK Must be coded as 0x00 Reserved for future use Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision "Note: 1	1D 00 00 00 00 00 00 00 00 00 00 00 00 00
92 93 94-127 128-191 192 193 194 195 196 197 198 199 200 201 202 203 200 201 202 203 204 205 206 207 206 207 206 207 206 207 206 209 210 211 211 212 211 211 212 214 215 216	SDRAM Read to Prechange Command Delay (RTP, RTP sir), Most Significant Byte SDRAM Read to Prechange Command Delay (RTP, RTP sir), Lower Clock Limit Reserved, Base Configuration Section Reserved, Base Configuration Section Reserved for hubre ise SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Device Revision Number PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Revision Number PMIC 1 Manufacturer ID Code, First Byte PMIC 1 Revision Number PMIC 1 Revision Number PMIC 2 Manufacturer ID Code, First Byte PMIC 2 Manufacturer ID Code, First Byte PMIC 1 Revision Number PMIC 1 Revision Number PMIC 2 Manufacturer ID Code, First Byte PMIC 2 Revision Number PMIC 3 Revision Number PMIC 4 Revision Number PMIC 4 Revision Number PMIC 5 Revision Number PMIC 5 Revision Number PMIC 7 Revision Number PMIC 7 Revision Number PMIC 8 Revision Number PMIC 8 Revision Number PMIC 9 Revision Number PMIC	12 nCK Must be coded as 0x00 Reserved for future use Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision "Note: 1	1D 000 000 000 000 000 000 000 000 000 0
92 93 94-127 128-191 192 193 194 195 196 197 198 200 201 202 203 200 200 200 200 200 200 200 200	SDRAM Read to Prechange Command Delay (RTP, RTP, sir), Most Significant Byte SDRAM Read to Prechange Command Delay (RTP, RTP, sir), Lower Clock Limit Reserved, Base Configuration Section Reserved for future use SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Device Type SPD Device Type SPD Device Type PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Revision Number PMIC 0 Revision Number PMIC 1 Manufacturer ID Code, Second Byte PMIC 1 Manufacturer ID Code, Second Byte PMIC 1 Device Type SPD Device Type SPD Device Type SPD Code, First Byte PMIC 1 Manufacturer ID Code, Second Byte PMIC 1 Manufacturer ID Code, Second Byte PMIC 1 Manufacturer ID Code, Second Byte PMIC 1 Manufacturer ID Code, First Byte PMIC 1 Device Type SPD Code, First Byte PMIC 1 Device Type SPD Code, First Byte PMIC 1 Manufacturer ID Code, First Byte PMIC 1 Manufacturer ID Code, First Byte PMIC 1 Manufacturer ID Code, First Byte PMIC 2 Manufacturer ID Code, Second Byte PMIC 2 Manufacturer ID Code, Second Byte Thermal Sensor Manufacturer ID Code, Second Byte PMIC Specification Level PMIC Specification Level	12 nCK Must be coded as 0x00 Reserved for future use Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision "Note: 1	1D 000 000 10 000 000 000 000 000 000 00



240	The Second second		
219	Is specification Level		
221,229	Demen Operation Center	Reserved	00
230	Transfer Water	30.00mm	05
231	Understanding interventional interventional intervention of the second	Front 1 < thickness < 2 mm	01
232	(Unbuffered): Reference Raw Card Used	Raw Card A Revision 0	00
233	(Unbuffered): DIMM Attributes	0 to +95 °C/2 row DRAM	82
		d Resident Reside	
234	(Unoumered: Module Organization	1 Package Ranks	00
235	Memory Channel Bus Width	2 channels/32 bits	22
236-239	Reserved	must be coded as 0x00	00
240-447	(Unbuffered)Module Type Specific Information	Reserved	00
448-509	Reserved for future use	*	00
510	CRC for Byte 0-509_Least Significant Byte	CRC	-
511	Like to Byte Unsugnedst significant Byte	CRC	-
512	Module Manuacturer ID Code, Hrst Byte	Advantech	04
513	Module Manuacturer ID Coop, second Byte	Distance D	6
514	Module Manufacturing Location	"Note: 2	
515	Module Manufacturing Late	"Note: 3 (Decimal)	
515	nedourin menunerizarring Ledo	"Note: + (Decimal)	
540			
510	Module Serial Number	"Note: 5 (Decimal)	
519			
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522			
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526			
527			
528			
529			
530			
531			
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535	Module Part Number	"Note: 6	
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550			-
551	Module Revision Code		00
552	DRVM Manufacturer ID Code, First Byte	Samsung	80
553	DRAH Manufacturer ID Code, Second Byte		CE
554	UPCAN Stopping	1994-7 T	35
555-639	Manufacturer's specific Lata	"Note: 7	-
640	Intel Extreme Memory Profile Identification String		00
641	Intel Externe Memory Profile Identification String		00
642	Intel Extreme Memory Profile Version		00
643	Intel Extreme Memory Profile Organization		00
644	Intel Extreme Memory Profile Configuration		r 00



645	RMC Vander ID	00
646	nino vandorio	00
647	namber of DAICo.	 00
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0+0	Print capacitities	 00
040-000	Ravu	 00
604		
655		00
656		 00
657		 00
658		00
659		00
660		00
661	Profile 1 String Name	00
662		00
663		00
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665		00
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668		00
669		00
670		 00
671		00
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673		00
674		00
675		00
676		00
677		00
678	Profile 2 String Name	00
679		00
680		00
681		00
682		00
683		00
684		00
695		 00
696		 00
600		
607		
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000		
690		
691		00
692		00
693	Profile 3 String Name	00
694		00
695		00
696		00
697		00
698		00
699		00
700		 00
701		 00
702	Cyclical Redundancy Code (CRC) for Base Configura tion Section, Least Significant Byte (for bytes 640–701)	00
703	Cyclical Redundancy Code (CRC) for Base Configura tion Section, Most Significant Byte (for bytes 640–701)	00
704	Profile 1 :Module VPP Voltage Level	00
705	Module VDD Voltage Level	00
706	Module VDDQ Voltage Level	00
707	Module TBD Voltage Level - THIS BYTE IS CURRENTLY RSVD	00
708	Memory Controller Voltage Level	00
709	SDRAM Minimum Cycle Time (ICKAVGmin) Least Significant Byte	00
710	SDRAM Minimum Cycle Time (ICKAVGmin).Most Significant Byte	00
711	SDRAM CAS Latencies Supported, First Byte	00
712	SDRAM CAS Latencies Supported Second Byte	00



713	SDRAM CAS Laborates Supported Third Bute		F 00
714	SUPONE CIS Laborate Supporte, mino pre		00
715	General Crist Latercles Supported Fibration		00
715	Scholar Crub Exercise Scholar Processor		
710	Rando in touring once Exercity SDRAM Ministrian CAS Laborat Time RAAmini Labort Stockforcet Bute		
710	Screen minimum CAS Example Time (Administrate diginicant of the SCREEN State)		
710	SDRAW Internet CAS Exempty Time (overninghost significant by/w SDRAW Internet CAS Exempty Time (overninghost significant by/w		
719	Software minimum PA's to CA's being time (excerning basis significant byte Software minimum PA's to CA's being time (excerning basis significant byte		
720	SUPAN MINIMUM PAS to CAS belay time (botching)Most significant Byte		
721	SUPPORT NUMBER OF PROVIDENT OF A CONTRACT OF A		
122	SUPAN MINIMUM KW Prechange Delay lime (PPPmin) Ander Signin can byte		
723	SUPAN Minimum Active to Prochage Delay Time (PASmin)Least significant Byte		00
724	SUPAN MINIMUM Active to Precharge Delay Time (Person plane) spin Cart Byte		00
725	SURAM Minimum Active to Active Remesh Delay Timetekomini Least Significant Byte		00
726	SURAM Minimum Active to Active Remest Delay Timetexcining Most significant Byte		
121	SURAM Minimum Winte Recovery Time (WHOMIN)LEAST Significant Byte		
728	SURAM MINIMUM WINE RECOVERY TIME (WHOMIN, MOST SIGNIFICANT BYRE		00
729	SURAM Minimum Renesh Recovery Delay Time(R-C-Timin Least significant Byte		00
730	SDRAM Minimum Refresh Recovery Dolay Time(RFCTmin) Most Significant Byte		00
731	SDRAM Minimum Refresh Recovery Dolay Time(RFC2min)Least Significant Byte		00
732	SDRAM Minimum Refresh Recovery Dolay Time(RFC2min) Most Significant Byte		00
733	SDRAM Minimum Refresh Recovery Delay Time(RFCsb)Least Significant Byte		00
734	SDRAM Minimum Refresh Recovery Delay Time(IRFCsbmin).Most Significant Byte		00
735-782	RSVD,must be coded as 0x00		00
763	Advanced Memory Overclocking Features		00
764	System CMD Rate Mode		00
765	Vendor Personality Byte - RSVD		00
766	Cyclical Redundancy Code (CRC) for Base Configura tion Section, Least Significant Byte(for bytes 704–765)		00
767	Cyclical Redundancy Code (CRC) for Base Configura tion Section, Most Signa Caar Byte for bytes 704–765		00
768	Profile2 :Module VPP Voltage Level		00
769	Module VDD Voltage Level		00
770	Module VDDQ Voltage Level		00
771	Module TBD Voltage Level - THIS BYTE IS CURRENTLY RSVD		00
	Memory Controller Voltage Level		
772	mentary consolier volage certer		00
772	SDRAM Minimum Cycle Time (tCKAVGmin),Least Significant Byte		00
772 773 774	SDRAM Minimum Cycle Time (ICKAVGmin),Least Significant Byte SDRAM Minimum Cycle Time (ICKAVGmin),Most Significant Byte		00
772 773 774 775	SDRAM Minimum Cycle Time (ICKAVGmin)Least Significant Byte SDRAM Minimum Cycle Time (ICKAVGmin).Most Significant Byte SDRAM CAS Latencies Supported.First Byte		00
772 773 774 775 776	SDRAM Minimum Cycle Time (ICKAVGmin)Least Significant Byte SDRAM Minimum Cycle Time (ICKAVGmin).Most Significant Byte SDRAM CAS Latencies Supported.First Byte SDRAM CAS Latencies Supported.Second Byte		00
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772 773 774 775 776 776 777 778 779	SDRAM Minimum Cycle Time (ICKAVGmin).Least Significant Byte SDRAM Minimum Cycle Time (ICKAVGmin).Most Significant Byte SDRAM CAS Latencies Supported,First Byte SDRAM CAS Latencies Supported,Second Byte SDRAM CAS Latencies Supported,Find Byte SDRAM CAS Latencies Supported,First Byte		00 00 00 00 00 00 00
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262Pin DDR5 5600 1.1V SO-DIMM 16GB Based on 2048Mx8 AQD-SD5V16GN56-SB

830	Cyclical Redundancy Code (CRC) for Base Configuration Section Least Stanificant Bytefor hyter 768–879)	00
831	Cyclical Redundancy Code (CRC) for Base Complete for Section Date Specificat System Code (CRC) for Base Complete for Section Date Specificat Date (Section 2014)	00
832	Contract researcy code (end) to date compare contracted most digenteent system operations.	00
833	I forma integrate (in the second se	00
834	Module VDF Volge Evel	00
835	Module TODA YONGGE CAVE Module TODA YONGGE CAVE	00
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937	memory contorner votage cerver	
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839	SDRAM CAS Laborate Supported Fart Bule	00
840	CREAM CASE Laterative Deported in the case	00
841	SDRAM CAS Latercies Supported Third Bute	00
842	SDRAM CAS Latencies Supported Fourth Byte	00
843	SDRAM CAS Latencies Supported Fifth Byte	00
844	RSVD for future CAS Latency	00
845	SDRAM Minimum CAS Latency Time (tAAmin)Least Significant Byte	00
846	SDRAM Minimum CAS Latency Time (XAAmin).Most Significant Byte	00
847	SDRAM Minimum RAS to CAS Delay Time (IRCDmin) Least Significant Byte	00
848	SDRAM Minimum RAS to CAS Delay Time (IRCDmin).Most Significant Byte	00
849	SDRAM Minimum Row Precharge Delay Time (tRPmin) Least Significant Byte	00
850	SDRAM Minimum Row Precharge Delay Time (RPmin),Most Significant Byte	00
851	SDRAM Minimum Active to Precharge Delay Time (IRASmin) Least Significant Byte	00
852	SDRAM Minimum Active to Precharge Delay Time (IRASmin).Most Significant Byte	00
853	SDRAM Minimum Active to Active/Refresh Delay Time(ROmin) Least Significant Byte	00
854	SDRAM Minimum Active to Active/Refresh Delay Time(tRCmin) Most Significant Byte	00
855	SDRAM Minimum Write Recovery Time (WRmin) Least Significant Byte	00
856	SDRAM Minimum Write Recovery Time (tWRmin),Most Significant Byte	00
857	SDRAM Minimum Refresh Recovery Delay Time(RFC1min)Least Significant Byte	00
858	SDRAM Minimum Refresh Recovery Delay Time(RFC1min)Most Significant Eyte	00
859	SDRAM Minimum Refresh Recovery Delay Time(RFC2min)Least Significant Byte	00
860	SDRAM Minimum Refresh Recovery Delay Time(RFC2min).Most Significant Byte	00
861	SDRAM Minimum Refresh Recovery Delay Time(RFCsb),Least Significant Byte	00
862	SDRAM Minimum Refresh Recovery Delay Time(RFCsbmin).Most Signi getift Bye	00
863-890	RSVD,must be coded as 0x00	00
891	Advanced Memory Overclocking Features	00
892	System CMD Rate Mode	00
893	Vendor Personality Byte - RSVD	 00
894	Cyclical Redundancy Code (CRC) for Base Configura tion Section, Least Significant Byte(for bytes 832–893)	00
895	Cyclical Redundancy Code (CRC) for Base Configura tion Section, Most Significant Byte(for bytes 832–893)	 00
896-1023	User Settings	00

Note :

- 1. Byte 194-201 -- By SPD_Hub & PMIC Vendor & Revision
- 1.1 Byte 194-197 RENESAS[(0x80), (0xB3), (0x80), (0x21)] ; MONTAGE[(0x86), (0x32), (0x80), (0x15)]
- 1.2 Byte 198-201 RENESAS[(0x80), (0xB3), (0x82), (0x20)] ; RICHTEK[(0x8A), (0x8C), (0x82), (0x11)] 2. Byte 514 -- Manufacturing location by manufacturing location
- 3. Byte 515 -- Module manufacturing date by year (YY). (Decimal)
- 4. Byte 516 -- Module manufacturing date by week (WW). (Decimal)
- 5. Bytes 517-520 -- Module Serial Number. (Decimal)
- 6. Bytes 521-550 -- Module Part Number. (ASCII format, unused digits are coded as ASCII blanks (0x20).
- 7. Bytes 552-553 -- DRAM Manufacturer ID Code by JEDEC definition. SAMSUNG :[(0x80) ,(0xCE)]
- 8. Bytes 555~639 -- These bytes are undefined and can be used own purpose