

# **Advantech**

# AQD-D5V32GN56-SB Datasheet

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## **ADVANTECH**

**Enabling an Intelligent Planet** 

#### 288Pin DDR5 5600 1.1V U-DIMM 32GB Based on 2048Mx8 AQD-D5V32GN56-SB

#### Description

AQD-D5V32GN56-SB is DDR5-5600(CL46)-45-45 SDRAM memory module. The SPD is programmed to JEDEC standard latency 5600Mbps timing of 46-45-45 at 1.1V. The module is composed of 16Gb CMOS DDR5 SDRAMs in FBGA package and one 8Kbit SPD Hub in 8pin TDFN package on a 288pin glass–epoxy printed circuit board.

The module is a Dual In-line Memory Module and intended for mounting onto 288 pins edge connector sockets. Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

#### Features

- RoHS compliant products.
- JEDEC standard 1.1V(1.067V~1.166V) Power supply
- VDDQ= 1.1V(1.067V~1.166V)
- VPP = 1.8V(+0.108V / -0.054V)
- Data transfer rates: PC5-5600
- Programmable CAS Latency: 22,26,28,30,32,36,40,42,46
- 16 bit pre-fetch
- Burst Length (BL) switch on-the-fly BL16 or BC8
- Bi-directional Differential Data-Strobe
- On Die Termination, Nominal, Park
- Serial presence detect hub (SPD Hub) with
   Integrated Temperature sensor
- Asynchronous reset
- PCB edge connector treated with 30u" Gold-Plating



Pin Name	Description	Pin Name	Description
CA[6:0]_A CA[6:0]_B	Address and Command Bus	DQ[31:0]_A DQ[31:0]_B	DIMM memory Data bus channel A & B
CS[1:0]_A CS[1:0]_B	Chip Select	CB[7:0]_A CB[7:0]_B	DIMM ECC Checkbits (CB) channel A & B
PAR_A PAR_B	Parity input	DQS[9:0]_A_t DQS[9:0]_B_t	Data Strobes (positive line of differential pair)
CK_t	Clocks (true/positive)	DQS[9:0]_A_c DQS[9:0]_B_c	Data Strobes (negative line of differential pair)
CK_c	Clocks (complement/negative)	TDQS[9:5]_A_t TDQS[9:5]_B_t	Not valid for x4 operation. Enabled via Mode Register.
ALERT_n	Alert for CRC error	TDQS[9:5]_A_c TDQS[9:5]_B_c	Not valid for x4 operation. Enabled via Mode Register.
RESET_n	Set DRAM to known state	VIN_BULK	DIMM Power Supply from system to PMIC
PCAMP	Control and Monitor Port	VIN_MGMT	DIMM Power Supply from system to PMIC
HSCL	I2C/I3C-Basic Host Sideband Bus Clock	VSS	Power supply return (ground)
HSDA	I2C/I3C-Basic Host Sideband Bus Data	RFU	Reserved for future use
HSA	I2C/I3C-Basic Host Sideband Bus Address	LBDQS	Loopback Data strobe output
LBDQ	Loopback Data output:		

#### 3



#### **Dimensions (Unit: millimeter)** Fron Pub Hub PMIC Back 133.35+0.45 5250+18 5.57 MAX 3.875 [153] 31.25<sup>+0.55</sup> [ 1230<sup>+22<sup>-</sup></sup> R0.80 [R31](2X) Hole [Ø59](4X) A В D 1.27±0.10 [50±4] nganananan (mi [6 VIEW E-E [2476] 57.80 [2276] 3.35 [132] 5.95 [234] 3.35 [132] 133.35 <u>36.08 [1420]</u> 9.35 [368] 30.22 [1190] 22.48 [885] 24.38 [960] 9.35 [368] 30 [1272] <u>8.50 [335</u> 28.90 [1138] 0.40 [803] 8.50 [335] 18 70 8.00 [315](2X) R0.65 [R263(8X) 3.00 [118](4X) 2.10 [83](4X) [575](2X) 4.60 0.60±0.03 [24±1] 3.85±0.10 [152±4] ω 2.10 0.85 [33] הההחחו 4.30 [169] 0.25 [10] 1.65 [65] 0.20 [8] 1.50±0.05 [59±2] Detail A Detail B 2.60 [102] [83] [83] Pin122 <u>2.10</u> Pin39 'in110 2.10 Pin51

Note:1. Tolerances on all dimensions +/-0.15mm unless otherwise specified.

0.25

2.60

С

Detail

0.25 [10]

0.50 [20]

Detail D

0.25 [10]

0.50 [2



## 288Pin DDR5 5600 1.1V U-DIMM 32GB Based on 2048Mx8 AQD-D5V32GN56-SB

#### **Pin Assignments**

		2	88-Pin DDR5	UDIN	AM Front			288-Pin DDR5 UDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VIN_BULK	37	DQ20_A	73	CK0_A_c	109	V <sub>SS</sub>	145	VIN_BULK	181	DQ22_A	217	CK1_A_c	253	Vss
2	NC/VIN_BULK	38	Vss	74	Vss	110	DQ5_B	146	VIN_BULK	182	Vss	218	Vss	254	DQ7_B
3	RFU	39	DQ21_A	75	RFU	111	V <sub>SS</sub>	147	PWR_GOO D	183	DQ23_A	219	RFU	255	V <sub>SS</sub>
4	HSCL	40	Vss	76	RFU	112	DQ8_B	148	HSA	184	Vss	220	RFU	256	DQ10_B
5	HSDA	41	DQ24_A	77	Vss	113	V <sub>SS</sub>	149	RFU	185	DQ26_A	221	V <sub>SS</sub>	257	Vss
6	Vss	42	Vss	78	CK0_B_t	114	DQ9_B	150	Vss	186	Vss	222	CK1_B_t	258	DQ11_B
7	RFU	43	DQ25_A	79	CK0_B_c	115	Vss	151	PWR_EN	187	DQ27_A	223	CK1_B_c	259	Vss
8	Vss	44	Vss	80	Vss	116	DM1_B_n	152	RFU	188	Vss	224	Vss	260	DQS1_B_c
9	DQ0_A	45	DM3_A_n	81	RFU	117	Vss	153	Vss	189	DQS3_A_c	225	RFU	261	DQS1_B_t
10	Vss	46	Vss	82	CA12_B	118	DQ12_B	154	DQ2_A	190	DQS3_A_t	226	RFU	262	Vss
11	DQ1_A	47	DQ28_A	83	Vss	119	Vss	155	Vss	191	Vss	227	Vss	263	DQ14_B
12	Vss	48	Vss	84	CA10_B	120	DQ13_B	156	DQ3_A	192	DQ30_A	228	CA11_B	264	Vss
13	DQS0_A_c	49	DQ29_A	85	CA8_B	121	VSS	157	V <sub>SS</sub>	193	V <sub>SS</sub>	229	CA9_B	265	DQ15_B
14	DQS0_A_t	50	Vss	86	Vss	122	DQ16_B	158	DM0_A_n	194	DQ31_A	230	Vss	266	Vss
15	Vss	51	CB0_A	87	CA6_B	123	V <sub>SS</sub>	159	V <sub>SS</sub>	195	V <sub>SS</sub>	231	CA7_B	267	DQ18_B
16	DQ4_A	52	Vss	88	CA4_B	124	DQ17_B	160	DQ6_A	196	CB2_A	232	CA5_B	268	Vss
17	Vss	53	CB1_A	89	Vss	125	V <sub>SS</sub>	161	V <sub>SS</sub>	197	V <sub>SS</sub>	233	V <sub>SS</sub>	269	DQ19_B
18	DQ5_A	54	Vss	90	CA2_B	126	DQS2_B_c	162	DQ7_A	198	CB3_A	234	CA3_B	270	Vss
19	Vss	55	DQS4_A_c	91	CA0_B	127	DQS2_B_t	163	Vss	199	Vss	235	CA1_B	271	DM2_B_n
20	DQ8_A	56	DQS4_A_t	92	Vss	128	Vss	164	DQ10_A	200	ALERT_n	236	Vss	272	Vss
21	Vss	57	Vss	93	CS0_B_n	129	DQ20_B	165	Vss	201	Vss	237	CS1_B_n	273	DQ22_B
22	DQ9_A	58	CS0_A_n	94	Vss	130	VSS	166	DQ11_A	202	CS1_A_n	238	Vss	274	Vss
23	Vss	59	Vss	95	RESET_n	131	DQ21_B	167	Vss	203	Vss	239	DQS4_B_c	275	DQ23_B
24	DM1_A_n	60	CA0_A	96	Vss	132	V <sub>SS</sub>	168	DQS1_A_c	204	CA1_A	240	DQS4_B_t	276	Vss
25	Vss	61	CA2_A	97	CB0_B	133	DQ24_B	169	DQS1_A_t	205	CA3_A	241	Vss	277	DQ26_B
26	DQ12_A	62	Vss	98	Vss	134	V <sub>SS</sub>	170	Vss	206	V <sub>SS</sub>	242	CB2_B	278	Vss
27	V <sub>SS</sub>	63	CA4_A	99	CB1_B	135	DQ25_B	171	DQ14_A	207	CA5_A	243	Vss	279	DQ27_B
28	DQ13_A	64	CA6_A	100	Vss	136	Vss	172	Vss	208	CA7_A	244	CB3_B	280	Vss
29	Vss	65	Vss	101	DQ0_B	137	DM3_B_n	173	DQ15_A	209	Vss	245	V <sub>SS</sub>	281	DQS3_B_c
30	DQ16_A	66	CA8_A	102	Vss	138	Vss	174	Vss	210	CA9_A	246	DQ2_B	282	DQS3_B_t
31	V <sub>SS</sub>	67	CA10_A	103	DQ1_B	139	DQ28_B	175	DQ18_A	211	CA11_A	247	V <sub>SS</sub>	283	Vss
32	DQ17_A	68	Vss	104	Vss	140	Vss	176	Vss	212	Vss	248	DQ3_B	284	DQ30_B
33	Vss	69	CA12_A	105	DQS0_B_c	141	DQ29_B	177	DQ19_A	213	RFU	249	Vss	285	Vss
34	DQS2_A_c	70	RFU	106	DQS0_B_t	142	Vss	178	Vss	214	RFU	250	DM0_B_n	286	DQ31_B
35	DQS2_A_t	71	Vss	107	Vss	143	RFU	179	DM2_A_n	215	Vss	251	Vss	287	Vss
36	Vss	72	CK0_A_t	108	DQ4_B	144	RFU	180	Vss	216	CK1_A_t	252	DQ6_B	288	RFU

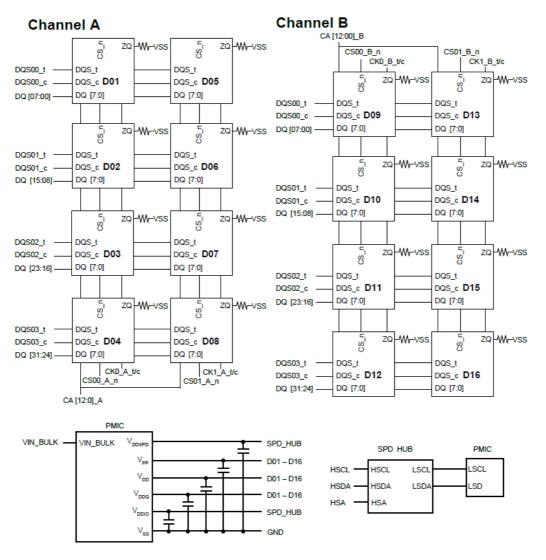
#### Notes:

Pin #2 is NC (No Connect) for JEDEC standard DDR5 modules. On non-standard modules used by enthusiasts that may require increased power supply, Pin #2 can be connected to VIN\_BULK rail on module.



#### **Function Block Diagram**

#### 2Rank, x8 DDR5 SDRAMs



Note 1: ZQ resistors are 240  $\Omega \pm 1\%$ .

This technical information is based on industry standard data and tests believed to be reliable. However, Advantech makes no warranties, either expressed or implied, as to its accuracy and assume no liability in connection with the use of this product. Advantech reserves the right to make changes in specifications at any time without prior notice.



#### 288Pin DDR5 5600 1.1V U-DIMM 32GB Based on 2048Mx8 AQD-D5V32GN56-SB

#### Operating Temperature Condition

	Parameter	Symbol	Rating	Unit	Note
Operat	ing Temperature	TOPER	0 to 85	°C	1,2
Note:	Operating Temperature is the case surface temperature on the center/to measurement conditions, please refer to JESD51-2 standard.	op side of th	ne DRAM. I	For the	

#### **Absolute Maximum DC Ratings**

Parameter	Symbol	Value	Unit	Note
Voltage on VDD relative to Vss	VDD	-0.3 ~ 1.4	V	1
Voltage on VDDQ pin relative to Vss	VDDQ	-0.3 ~ 1.4	V	1
Voltage on any pin relative to Vss	VIN, VOUT	-0.3 ~ 1.4	V	1
Storage temperature	TSTG	-55~+100	°C	1,2

Note: 1. Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

#### AC & DC Operating Conditions

#### **Recommended DC operating conditions**

Parameter	Symphol	Voltage		l lmit	Notes		
Farameter	Symbol	Symbol Voltage		Тур.	Мах	Unit	Notes
Host Supply Voltage	VIN_BULK	12.0	4.25	5.0	5.5	V	
PMIC Output Supply Voltage	VDD	1.1	1.067	1.1	1.166	V	1,2,3
PMIC Output Supply Voltage	VDDQ	1.1	1.067	1.1	1.166	V	1,2,3
PMIC Output Supply Voltage	VPP	1.8	1.746	1.8	1,908	V	3
AC Input Logic High	VIH(AC)	TBD	-	-	-	mV	
AC Input Logic Low	VIL(AC)	TBD	-	-	-	mV	
DC Input Logic High	VIH(DC)	TBD	-	-	-	mV	
DC Input Logic Low	VIL(DC)	TBD	-	-	-	mV	

Note: (1) VDD must be within 66mv of VDDQ

(2) AC parameters are measured with VDD and VDDQ tied together.

(3) This includes all voltage noise from DC to 2 MHz at the DRAM package ball.



## IDD Specification parameters Definition - 32GB

Symbol	Condition	32GB	Unit
IDD0	One bank ACTIVATE-PRECHARGE current	TBD	mA
IDD0F	Operating Four Bank Active-Precharge Current	TBD	mA
IDD2N	Precharge Standby Current	TBD	mA
IDD2P	Precharge Power-Down Current	TBD	mA
IDD3N	Active standby current	TBD	mA
IDD3P	Active Power-Down Current	TBD	mA
IDD4R	Burst Read Current	TBD	mA
IDD4W	Burst write current	TBD	mA
IDD5B	Burst Refresh Current (1x REF)	TBD	mA
IDD5C	Burst Refresh Current (Same Bank Refresh Mode)	TBD	mA
IDD6N	Self refresh current: Normal temperature range (0–85°C)	TBD	mA
IDD7	Bank interleave read current	TBD	mA
IDD8	Maximum power-down current	TBD	mA



Timing Param	eters & Sp	ecificatio	ons						
_		DDR5	-4800	DDR5	-5600	DDR5	DDR5-6400		
Parameter	Symbol	Min	Мах	Min	Мах	Min	Мах	Unit	Notes
			Clock	Timing					
Clock period average	tCK (AVG)	0.416	<0.454	0.357	<0.384	0.312	<0.333	ns	1
Command and Address Timing									
Read to Read command delay for same bank group	tCCD_L	max(8nCK, 5ns)	_	max(8nCK, 5ns)	-	max(8nCK, 5ns)	-	nCK,ns	8
Write to Write command delay for same bank groupp	tCCD_L_WR	max(32nCK, 20ns)	_	max(32nCK, 20ns)	_	max(32nCK, 20ns)	_	nCK,ns	8
Write to Write command delay for same bank group, second write not RMW	tCCD_L_WR2	max(16nCK, 10ns)	_	max(16nCK, 10ns)	_	max(16nCK, 10ns)	_	nCK,ns	8
Read to Write command delay for same bank group	tCCD_L_RTW		CL - CV	/L + RBL/2 + 2tC + (tRPST - 0.5td		S offset)		nCK,ns	3,5,6,8
Write to Read command delay for same bank group	tCCD_L_WTR		C	WL + WBL/2 + M	ax(16nCK,10n	5)		nCK,ns	4,6,8
Read to Read command delay for different bank group	tCCD_S	8	-	8	-	8	-	nCK	8
Write to Write command delay for different bank group	tCCD_S_WR	8	_	8	_	8	_	nCK	8
Read to Write command delay for different bank group	tCCD_S_RTW	CL - CV	VL + RBL/2 + 2	tCK - (Read DQS	S offset) + (tRP	ST - 0.5tCK) + t	WPRE	nCK,ns	3,5,6,8
Write to Read command delay for different bank group	tCCD_S_WTR		С	WL + WBL/2 + N	lax(4nCK,2.5ns	3)		nCK,ns	4,6,8
Write to Read with Auto Precharge command delay for same bank	tCCD_WTRA			CWL + WBL/2 ·	+ tWR - tRTP			nCK,ns	2,4,6,8



		DDR5-4800		DDR5-5600		DDR5-6400				
Parameter	Symbol	Min	Max	Min Max		Min	Max	Unit	Notes	
Activate to Activate command delay to same bank group for 1KB page size	tRRD_L(1K)	max(8nCK, 5ns)	_	max(8nCK, 5ns)	_	max(8nCK, 5ns)	_	nCK,ns	8	
Activate to Activate command delay to same bank group for 2KB page size	tRRD_L(2K)	max(8nCK, 5ns)	_	max(8nCK, 5ns)	_	max(8nCK, 5ns)	_	nCK,ns	8	
Activate to Activate command delay to different bank group for 1KB page size	tRRD_S(1K)	8	_	8	_	8	_	nCK	8	
Activate to Activate command delay to different bank group for 2KB page size	tRRD_S(2K)	8	_	8	_	8	_	nCK	8	
Four activate window for 1KB page size	tFAW (1K)	Max(32nCK, 13.333ns)	-	Max(32nCK, 11.428ns)	-	Max(32nCK, 10.000ns)	-	nCK,ns		
Four activate window for 2KB page size	tFAW (2K)	Max(40nCK, 16.666ns)	_	Max(40nCK, 14.285ns)	_	Max(40nCK, 12.500ns)	-	nCK,ns		
Read to Precharge command delay	tRTP	Max(12nCK, 7.5ns)	_	Max(12nCK, 7.5ns)	_	Max(12nCK, 7.5ns)	_	nCK,ns	8	
Precharge to Precharge command delay	tPPD	2	-	2	-	2	-	nCK	7,8	
Write recovery time	tWR	30	-	30	-	30	-	ns	8	



#### Notes:

- 1. tCK(avg)min listed for reference only, refer to the Speed Bins and Operations section which lists all valid tCK(avg) values.
- 2. tCCD\_WTRA(min) shall always be greater than or equal to CWL + WBL/2 + tWR(min) tRTP(min), and when using the appropriate rounding algorithms,

nCCD\_WTRA(min) shall always be greater than or equal to CWL + WBL/2 + nWR(min) - nRTP(min).

- 3. RBL: Read burst length associated with Read command
  - RBL = 32 (36 w/ RCRC on) for fixed BL32 and BL32 in BL32 OTF mode
  - RBL = 16 (18 w/ RCRC on) for fixed BL16 and BL16 in BL32 OTF mode
  - RBL = 16 (18 w/ RCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode

4. WBL: Write burst length associated with Write command

WBL = 32 (36 w/ WCRC on) for fixed BL32 and BL32 in BL32 OTF mode

WBL = 16 (18 w/ WCRC on) for fixed BL16 and BL16 in BL32 OTF mode

WBL = 16 (18 w/ WCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode

5.5 - The following is considered for tRTW equation

1tCK needs to be added due to tDQS2CK

Read DQS offset timing can pull in the tRTW timing

1tCK needs to be added when 1.5tCK postamble

- 6. CWL=CL-2
- 7. tPPD applies to any combination of precharge commands (PREab, PREsb, PREpb). tPPD also applies to any combination of precharge commands to a different die in a

3DS DDR5 SDRAM.

8. This parameter only specifies minimum values (there is no maximum value). The maximum value cells have been merged in

the table to improve legibility.



## 288Pin DDR5 5600 1.1V U-DIMM 32GB Based on 2048Mx8 AQD-D5V32GN56-SB

## SERIAL PRESENCE DETECT SPECIFICATION

Byte	Function Described	-	iction	HEX
0 N	umber of Bytes in SPD Device	SPD Total	: 1024Bytes	r -
1 S	PD Revision for Base Configuration Parameters	Vers	ion 1.1	
2 K	ey Byte / Host Bus Command Protocol Type	DDR5	SDRAM	
3 К	ey Byte / Module Type		DIMM	
4 FI	rst SDRAM Density and Package	Monolithic SDRAM	16Gb	
5 FI	rst SDRAM Addressing	Row : 16	Column : 10	
6 FI	rst SDRAM I/O Width		x8	
7 FI	rst SDRAM Bank Groups & Banks Per Bank Group	8 bank groups/4 b	anks per bank group	
8 S	econd SDRAM Density and Package			
9 S	acond SDRAM Addressing			
10 S	econdary SDRAM I/O Width			
11 S	acond SDRAM Bank Groups & Banks Per Bank Group			
12 S	DRAM BL32 & Post Package Repair	One repair element per bank group	Burst length 32 supported	
3 S	DRAM Duty Cycle Adjuster & Partial Array Self Refresh	Device supports DCA to	r 4-phase internal clock(s)	
4 S	DRAM Fault Handling		ision control in MR9	
_	aserved a		ded as 0x00	
_	DRAM Nominal Voltage, VDD	Operable:1.1V	Endurant:1.1V	
_	DRAM Nominal Voltage, VDDQ	Operable:1.1V	Endurant:1.1V	
	DRAM Nominal Voltage, VPP	Operable:1.8V	Endurant:1.8V	
_	RAM Timing		ings per JESD79-5	
_	DRAM Minimum Cycle Time (tCKAVGmin), Least Significant Byte	water name to be the UTI	and the second second	
	DRAM Minimum Cycle Time (CKAVGmin), Csart diginitari Cyte	357	7 ps	
	DRAM Maximum Cycle Time (ICKAVGmax), Least Significant Byte			+
	DRAM Maximum Cycle Time (ICKAVGmax), Most Significant Byte	1010	ps (	
_	DRAM CAS Latencies Supported:First Byte	01.00.00	5,28,30,32	+
_	DRAM CAS Latencies Supported:Second Byte		0,42,46,50	+
-		UL,30,41	0,42,40,50	
_	DRAM CAS Latencies Supported:Third Byte		•	
	DRAM CAS Latencies Supported Fourth Byte			
	DRAM CAS Latencies Supported Fifth Byte		*	-
	eserved	must be co	ded as 0x00	-
_	DRAM Minimum CAS Latency Time (tAAmin), Least Significant Byte	1600	) ps	<u> </u>
_	DRAM Minimum CAS Latency Time (tAAmin), Most Significant Byte			-
_	DRAM Minimum RAS to CAS Delay Time (RCDmin), Least Significant Byte	1600	) ps	
_	DRAM Minimum RAS to CAS Delay Time (RCDmin), Most Significant Byte			-
_	DRAM Minimum Row Precharge Delay Time (tRPmin), Least Significant Byte	1600	) os	
_	DRAM Minimum Row Precharge Delay Time (IRPmin), Most Significant Byte			_
_	DRAM Minimum Active to Precharge Delay Time (IRASmin), Least Significant Nibble	3200	) os	
	DRAM Minimum Active to Precharge Delay Time (RASmin), Most Significant Byte		- P.3	
8 S	DRAM Minimum Active to Active/Refresh Delay Time (RCmin), Least Significant Nibble	4800	-	
9 S	DRAM Minimum Active to Active/Refresh Delay Time (IRCmin), Most Significant Nibble	-000	, pa	
0 S	DRAM Minimum Write Recovery Time (tWRmin), Least Significant Nibble	- 3000		
1 S	DRAM Minimum Write Recovery Time (tWRmin), Most Significant Nibble	3000	- P.0	
2 S	DRAM Minimum Refresh Recovery Delay Time (IRFC1 min, IRFC1 sir min).Least Significant Byte		5 ns	
3 S	DRAM Minimum Refresh Recovery Delay Time (IRFC1 min, IRFC1 sir min),Most Significant Byte	230	112	
4 S	DRAM Minimum Refresh Recovery Delay Time (IRFC2min, IRFC2 sir min),Least Significant Byte			
5 S	DRAM Minimum Refresh Recovery Delay Time (IRFC2min, IRFC2 sir min),Most Significant Byte	160	) ns	
	DRAM Minimum Refresh Recovery Delay Time (IRFCsbmin, IRFCsb sir min)Least Significant Byte			
	DRAM Minimum Refresh Recovery Delay Time (IRFCsbmin, IRFCsb sirmin).Most Significant Byte	130	) ns	
_	DRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(RFC1 dir min) Least Significant Byte			
	DRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(RFC1 dir min),Most Significant Byte	manalithi	c SDRAMs	
_	DRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(tRFC2 dir min)Least Significant Byte			
_	DRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(RRC2 dir min).Most Significant Byte	manalithi	c SDRAMs	
	ORAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(RRCsb dir min) Least Significant Byte			
_	DRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(RFCsb dir min),Most Significant Byte	monolithi	c SDRAMs	
_	DRAM Refresh Management, First Byte, First SDRAM			
	DRAM Refresh Management, First Byte, First SURAM DRAM Refresh Management, Second Byte, First SDRAM	+		
_	URAM Refresh Management, Second Byte, First SURAM DRAM Refresh Management, First Byte, Second SDRAM	+		
-	URAM Remesh Management, First Byte, Second SURAM DRAM Refresh Management, Second Byte, Second SDRAM			
_				
N 18	DRAM Adaptive Refresh Management, First SDRAM, First Byte,Level A			_
_	DRAM Adaptive Refresh Management, First SDRAM, Second Byte, Level A			



61	SDRAM Adaptive Refresh Management, Second SDRAM, Second Byte,Level A		<b>r</b> 00
	SDRAM Adaptive Refresh Management, First SDRAM, First Byte Level B		00
63	SDRAM Adaptive Retresh Management, First SDRAM, Second Byte,Level B		00
64	SDRAM Adaptive Refresh Management, Second SDRAM, First Byte,Level B		00
65	SDRAM Adaptive Refresh Management, Second SDRAM, Second Byte,Level B		00
66	SDRAM Adaptive Refresh Management, First SDRAM, First Byte,Level C		00
67	SDRAM Adaptive Refresh Management, First SDRAM, Second Byte,Level C		00
68	SDRAM Adaptive Refresh Management, Second SDRAM, First Byte,Level C		00
69	SDRAM Adaptive Refresh Management, Second SDRAM, Second Byte,Level C		00
70	SDRAM Minimum Active to Active Command Delay Time, Same Bank Group,(IRRD Lmin),Least Significant Byte	5000 ps	8
71	SDRAM Minimum Active to Active Command Delay Time, Same Bank Group,(IRRD Lmin),Most Significant Byte	0000 pa	18
72	SDRAM Minimum Active to Active Command Delay Time, Same Bank Group,(IRRD Lmin),Lower Clock Limit	8 nCK	00
	SDRAM Minimum CAS in to CAS in Command Delay Time, Same Bank Group,(ICCD Lmin),Least Significant Byte	5000 ps	8
74	SDRAM Minimum CAS in to CAS in Command Delay Time, Same Bank Group,(tCCD Lmin),Most Significant Byte		1
	SDRAM Minimum CAS in to CAS in Command Delay Time, Same Bank Group,(ICCD Lmin),Lower Clock Limit	8 nCK	00
	SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (tCCD L. WRmin),Least Significant Byte	20000 ps	20
	SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (tCCD L. WRmin),Most. Significant Byte	-	48
	SDRAM Minimum Write CAS n to Write CAS n Command Delay Time, Same Bank Group (tCCD L WRmin),Lower Clock Limit	32 nCK	20
	SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (CCD L. WR2min)Least Significant Byte	10000 ps	10
	SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (tCCD L. WR2min),Most Significant Byte		27
	SDRAM Minimum Write CAS n to Write CAS n Command Delay Time, Same Bank Group (CCD L WR2min) Lower Clock Limit	16 nCK	10
	SDRAM Minimum Four Activate Window (tFAWmin) Least Significant Byte	11428 ps	20
	SDRAM Minimum Four Activate Window (tFAWmin) Most Significant Byte		
	SDRAM Minimum Four Activate Window (FAWmin)Lower Clock Limit SDRAM With the Rend Command Delay, for Some Back, Group (CCC) 1, WTRNLeast, Step/Renet Rule	32 nCK	20
	SDRAM Write to Read Command Delay for Same Bank Group (CCD L WTR) Least Significant Byte	10000 ps	21
	SDRAM Write to Read Command Delay for Same Bank Group (tCCD L WTR), Most Significant Byte	40 -04	10
	SDRAM Write to Read Command Delay for Same Bank Group (ICCD L WTR),Lower Clock Limit SDRAM Write to Read Command Delay for Different Bank Group (ICCD S WTR), Least Significant Byte	16 nCK	C4
	SDRAM Write to Read Command Delay for Different Bank Group (CCD S WTR), Least Significant Byte SDRAM Write to Read Command Delay for Different Bank Group (CCD S WTR), Most Significant Byte	2500 ps	05
	SDRAM Write to Read Command Delay for Different Bank Group (ICCD S WTR), head argumetant by a	4 nCK	04
	SDRAM Read to Precharge Command Delay (RTP, IRTP, sir), Least Significant Byte	4 165	40
	SDRAM Read to Precharge Command Dalay (RTP, RTP sir), Most Significant Byte	7500 ps	10
	SRAM Read to Procharge Command Delay (RTP, RTP sir), Lower Clock Limit	12 nCK	00
	Reserved, Base Configuration Section	Must be coded as 0x00	00
	Reserved for future use	Reserved for future use	
		Reserved for future use Version 1.0	00
192	Reserved for future use SPD Revision for Module Information Hashing Sequence	Reserved for future use Version 1.0 No authentication	
192 193	SPD Revision for Module Information	Version 1.0	00
192 193 194	SPD Revision for Module Information Hashing Sequence	Version 1.0	00
192 193 194 195	SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte	Version 1.0	00
192 193 194 195 196	SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Manufacturer ID Code, Second Byte	Version 1.0 No authentication	00
192 193 194 195 196 197	SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Manufacturer ID Code, Second Byte SPD Device Type SPD Device Revision Number	Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision	00
192 193 194 195 196 197 198	SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Device Type SPD Device Revision Number PMIC 0 Manufacturer ID Code, First Byte	Version 1.0 No authentication	00
192 193 194 195 196 197 198 199	SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Manufacturer ID Code, Second Byte SPD Device Type SPD Device Revision Number PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Manufacturer ID Code, Second Byte	Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision	00
192 193 194 195 196 197 198 199	SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Device Type SPD Device Revision Number PMIC 0 Manufacturer ID Code, First Byte	Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision	00
192 193 194 195 196 197 198 199 200	SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Manufacturer ID Code, Second Byte SPD Device Type SPD Device Revision Number PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Manufacturer ID Code, Second Byte	Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision	00
192 193 194 195 196 197 198 199 200 201	SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Manufacturer ID Code, Second Byte SPD Device Revision Number PMIC 0 Manufacturer ID Code, Second Byte PMIC 0 Manufacturer ID Code, Second Byte PMIC 0 Device Type	Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision	0
192 193 194 195 196 197 198 199 200 201 202	SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Davice Type SPD Device Revision Number PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Manufacturer ID Code, Second Byte PMIC 0 Device Type PMIC 0 Device Type	Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision	0
192 193 194 195 196 197 198 199 200 201 202 203	SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Davice Type SPD Device Revision Number PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Manufacturer ID Code, Second Byte PMIC 0 Device Type PMIC 0 Revision Number PMIC 1 Manufacturer ID Code, First Byte	Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision	
192 193 194 195 196 197 198 199 200 201 202 203 203 204	SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Device Type SPD Device Revision Number PMIC 0 Manufacturer ID Code, Second Byte PMIC 0 Manufacturer ID Code, Second Byte PMIC 0 Device Type PMIC 0 Device Type PMIC 1 Manufacturer ID Code, First Byte PMIC 1 Manufacturer ID Code, Second Byte	Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision	0
192 193 194 195 196 197 198 199 200 201 202 203 204 205	SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Manufacturer ID Code, Second Byte PD Device Type PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Manufacturer ID Code, Second Byte PMIC 0 Device Type PMIC 0 Device Type PMIC 0 Revision Number PMIC 1 Manufacturer ID Code, First Byte PMIC 1 Manufacturer ID Code, Second Byte	Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision	
192 193 194 195 196 197 198 199 200 201 202 203 204 205 206 207	SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Manufacturer ID Code, Second Byte SPD Device Type PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Manufacturer ID Code, Second Byte PMIC 0 Device Type PMIC 1 Manufacturer ID Code, Second Byte PMIC 1 Manufacturer ID Code, First Byte PMIC 1 Manufacturer ID Code, First Byte PMIC 1 Manufacturer ID Code, Second Byte PMIC 1 Manufacturer ID Code, First Byte PMIC 2 Manufacturer ID Code, First Byte PMIC 2 Manufacturer ID Code, Second Byte PMIC 2 Manufacturer ID Code, First Byte PMIC 2 Manufacturer ID Code, Second Byte PMIC 2	Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision	
192 193 194 195 196 197 198 199 200 201 202 203 204 205 206 207	SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Manufacturer ID Code, Second Byte SPD Device Type SPD Device Type PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Revision Number PMIC 1 Manufacturer ID Code, Second Byte PMIC 2 Manufacturer ID Code, Second Byte PMIC 2 Manufacturer ID Code, First Byte PMIC 2 Manufacturer ID Code, First Byte PMIC 4 Manufacturer ID Code, Second Byte PMIC 4 Manufacturer ID	Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision	
192 193 194 195 196 197 198 199 200 201 202 203 204 205 206 207 208	SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Manufacturer ID Code, Second Byte SPD Device Type PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Manufacturer ID Code, Second Byte PMIC 0 Device Type PMIC 1 Manufacturer ID Code, Second Byte PMIC 1 Manufacturer ID Code, First Byte PMIC 1 Manufacturer ID Code, First Byte PMIC 1 Manufacturer ID Code, Second Byte PMIC 1 Manufacturer ID Code, First Byte PMIC 2 Manufacturer ID Code, First Byte PMIC 2 Manufacturer ID Code, Second Byte PMIC 2 Manufacturer ID Code, First Byte PMIC 2 Manufacturer ID Code, Second Byte PMIC 2	Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision	
192 193 194 195 196 197 198 199 200 201 200 201 202 203 204 205 206 207 208 209 210	SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Device Type SPD Device Type PMIC 0 Manufacturer ID Code, First Byte PMIC 1 Manufacturer ID Code, First Byte PMIC 1 Manufacturer ID Code, First Byte PMIC 1 Revision Number PMIC 2 Manufacturer ID Code, First Byte PMIC 2 Manufacturer I	Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision	
192 193 194 195 196 197 198 199 200 201 202 203 204 205 206 207 208 209 210 211	SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Device Type SPD Device Type PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Manufacturer ID Code, First Byte PMIC 1 Manufacturer ID Code, First Byte PMIC 2 Manufacturer ID Code, First Byte PMIC 3 Revision Number PMIC 3 Revision Number PMIC 4 Manufacturer ID Code, First Byte PMIC 5 Revision Number PMIC 5 Revision Number PMIC 6 Revision Number PMIC 7 Device Type PMIC 7 Revision Number PMIC 8 Revision Number PMIC 8 Revision Number PMIC 9 Revision Number PMIC	Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision	
192 193 194 195 196 197 198 200 201 202 203 204 205 206 207 208 206 207 208 209 210 211 212	SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Manufacturer ID Code, Second Byte SPD Device Revision Number PMIC 0 Manufacturer ID Code, Second Byte PMIC 0 Manufacturer ID Code, Second Byte PMIC 0 Revision Number PMIC 1 Manufacturer ID Code, First Byte PMIC 2 Manufacturer ID Code, First Byte PMIC 2 Revision Number PMIC 3 Revision Number PMIC 3 Revision Number PMIC 4 Revision Number PMIC 4 Revision Number PMIC 5 Revision Number PMIC 5 Revision Number PMIC 7 Revision Number PMIC 7 Revision Number PMIC 7 Revision Number PMIC 7 Revision Number PMIC 8 Revision Number PMIC 8 Revision Number PMIC 9 Revision Number	Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision	
192 193 194 195 196 197 198 199 200 201 202 203 204 205 206 207 208 209 210 211 212 213	SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Manufacturer ID Code, First Byte SPD Device Type SPD Device Revision Number PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Device Type PMIC 0 Revision Number PMIC 1 Manufacturer ID Code, First Byte PMIC 1 Device Type PMIC 1 Revision Number PMIC 1 Revision Number PMIC 2 Manufacturer ID Code, First Byte PMIC 2 Revision Number PMIC 3 Revision Number PMIC 3 Revision Number PMIC 4 Revision Number PMIC 4 Revision Number PMIC 5 Revision Number PMIC 5 Revision Number PMIC 7 Revision Number PMIC 7 Revision Number PMIC 8 Revision Number PMIC 8 Revision Number PMIC 9 Revision	Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision	
192 193 194 195 196 197 198 199 200 201 202 203 204 205 205 205 205 206 207 208 209 210 211 212 213 214	SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Device Type SPD Device Type PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Manufacturer ID Code, First Byte PMIC 1 Manufacturer ID Code, First Byte PMIC 1 Revision Number PMIC 1 Revision Number PMIC 1 Revision Number PMIC 2 Manufacturer ID Code, First Byte PMIC 2 Manufacturer ID Code, First Byte PMIC 2 Revision Number PMIC 3 Revision Number PMIC 4 Revision Number PMIC 4 Revision Number PMIC 4 Revision Number PMIC 5 Revision Number	Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision	
192 193 194 195 196 197 198 200 201 202 203 204 205 206 207 208 209 210 211 212 213 214 215	SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Device Type SPD Device Type PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Revision Number PMIC 0 Revision Number PMIC 1 Manufacturer ID Code, First Byte PMIC 2 Manufacturer ID Code, First Byte PMIC 2 Manufacturer ID Code, First Byte Themal Sensor Manufacturer ID Code, Second Byte PMIC 3 Manufacturer ID Code, Second Byte PMIC 2 Manufacturer ID Code, First Byte PMIC 2 Manufacturer ID Code, First Byte PMIC 2 Manufacturer ID Code, Second	Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision	
192 193 194 195 196 197 198 200 201 202 203 204 205 205 206 207 208 205 206 207 208 209 210 211 211 212 213 214 215 216	SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Device Revision Number PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Manufacturer ID Code, First Byte PMIC 1 Manufacturer ID Code, First Byte PMIC 1 Manufacturer ID Code, Second Byte PMIC 1 Manufacturer ID Code, First Byte PMIC 1 Manufacturer ID Code, First Byte PMIC 2 Revision Number PMIC 2 Revision Manufacturer ID Code, Second Byte PMIC 3 Manufacturer ID Code, First Byte Thermal Sensor Manufacturer ID Code, Second Byte PMIC 4 Manufacturer ID Code, Second Byte PMIC 4 Manufacturer ID Code, Second Byte PMIC 5 Revision Number PMIC 5 Revision Number PMIC 7 Manufacturer ID Code, Second Byte PMIC 7 Manuf	Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision	
192 193 194 195 196 197 198 200 201 202 203 204 205 206 207 208 206 207 208 209 210 211 211 212 213 214 215 216 217	SPD Revision for Module Intornation Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Davice Type SPD Device Type PMIC 0 Manufacturer ID Code, Second Byte PMIC 0 Manufacturer ID Code, Second Byte PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Revision Number PMIC 1 Manufacturer ID Code, First Byte PMIC 1 Device Type PMIC 1 Device Type PMIC 1 Revision Number PMIC 1 Revision Number PMIC 2 Manufacturer ID Code, First Byte PMIC 2 Revision Number PMIC	Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision	
192 193 194 196 197 198 199 200 201 202 203 204 205 206 205 206 205 206 200 210 211 212 213 214 215 216 217 218	SPD Revision for Module Information Hashing Sequence SPD Manufacturer ID Code, First Byte SPD Device Revision Number PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Manufacturer ID Code, First Byte PMIC 0 Manufacturer ID Code, First Byte PMIC 1 Manufacturer ID Code, First Byte PMIC 1 Manufacturer ID Code, Second Byte PMIC 1 Manufacturer ID Code, First Byte PMIC 1 Manufacturer ID Code, First Byte PMIC 2 Revision Number PMIC 2 Revision Manufacturer ID Code, Second Byte PMIC 3 Manufacturer ID Code, First Byte Thermal Sensor Manufacturer ID Code, Second Byte PMIC 4 Manufacturer ID Code, Second Byte PMIC 4 Manufacturer ID Code, Second Byte PMIC 5 Revision Number PMIC 5 Revision Number PMIC 7 Manufacturer ID Code, Second Byte PMIC 7 Manuf	Version 1.0 No authentication By SPD_Hub & PMIC Vendor & Revision	



221-229	Reserved	Reserved	00
230	(Unbuffered): Module Nominal Height	31.25mm	11
231	(Unbuffered): Module Maximum Thickness	Front,1 < thickness < 2 mm,Back	11
232	(Unbuffered): Reference Raw Card Used	Raw Card B Revision 0	01
233	(Unbuffered): DIMM Attributes	0 to +95 °C/1 row DRAM	81
		2 Package Ranks	
234	(Unbuffered): Module Organization	2 Package Banks	08
235	Memory Channel Bus Width	2 channels/32 bits	22
236-239	Reserved	must be coded as 0x00	00
240-447	(Unbuffered):Module Type Specific Information	Reserved	00
448-509	Reserved for future use	*	00
510	CRC for Byte 0–509,Least Significant Byte	CRC	-
511	CRC for Byte 0-509,Most Significant Byte	CRC	-
512	Module Manufacturer ID Code, First Byte	1 download	8A
513	Module Manufacturer ID Code, Second Byte	Advantech	C8
514	Module Manufacturing Location	"Note: 2	-
515	Module Manufacturing Date	"Note: 3 (Decimal)	-
	Module Manufacturing Date	"Note: 4 (Decimal)	-
517			-
518			-
519	Module Serial Number	"Note: 5 (Decimal)	-
520			-
521			-
522			-
523			
524			-
525			
526			-
527			
528			
529			
530 531			
532			
533			
534			
535	Module Part Number	"Note: 6	
536			
537			
538			
539			-
540			
541			-
542			
543			-
544			-
545			-
546			-
547			-
548			-
549			-
550	1		-
551	Module Revision Code		00
552	DRAM Manufacturer ID Code, First Byte		80
	DRAM Manufacturer ID Code, Second Byte	Samsung	CE
	DRAM Stopping		95
	Manufacturer's Specific Data	"Note: 7	00
	Intel Extremo Memory Profile Identification String	(1986) - 8	00
	Intel Extreme Memory Profile Identification String		00
642	Intel Externe Memory Profile Version		00
	Intel Externe Memory Profile Organization		00
644	Intel Extreme Memory Profile Configuration	1	00
		l	00
	PMIC Vendor ID PMIC Vendor ID		00



647	Number of PMICs	00
648	PMIC Capabilities	00
	RSVD	00
654		00
655		00
656		00
657		00
658		00
659		00
660		00
661		00
662	Profile 1 String Name	00
663		00
664		00
665	Profile 1 String Name 第3頁	00
666		00
667		00
668		00
669		00
670		00
671		00
672		00
673		00
674		00
675		00
676		00
677		00
678	Profile 2 String Name	00
679		00
680		00
681		00
682		00
683		00
684		00
685		00
686		00
687		00
688		00
689		00
690		00
691		00
692		00
693	Profile 3 String Name	00
694		00
695		00
696		00
697		00
698		00
699		00
700		00
701		00
702	Overlial Redundancy Code (CRC) for Base Configura tion Section, Least Significant Byte (for bytes 640–701)	00
703	Overlial Redundancy Code (CRC) for Base Configura tion Section, Most Significant Byte (for bytes 640-701)	00
704	Profile 1 :Module VPP Voltage Level	00
705	Module VDD Voltage Level	00
706	Module VDDQ Voltage Level	00
707	Module TBD Voltage Level - THIS BYTE IS CURRENTLY RSVD	00
708	Memory Controller Voltage Level	00
709	SDRAM Minimum Cycle Time (ICKAVGmin),Least Significant Byte SDRAM Minimum Cycle Time (ICKAVGmin),Most Significant Byte	00
710		00
712	SDRAM CAS Latencies Supported,First Byte SDRAM CAS Latencies Supported,Second Byte	00
	SURAM CAS Latencies Supported, Second Byte SDRAM CAS Latencies Supported, Third Byte	00
	SDRAM CAS Latencies Supported, Hind Byte	00

# **AD\ANTECH**

#### Enabling an Intelligent Planet

111     DNU Col Lances Science XPR By     Image: Col Lances Science XPR By       112     DRU Minue Col Lances Tes (Notes) Aug     Image: Col Lances Tes (Notes) Aug     Image: Col Lances Tes (Notes) Aug       113     DRU Minue Col Lances Tes (Notes) Aug     Image: Col Lances Tes (Notes) Aug     Image: Col Lances Tes (Notes) Aug       113     DRU Minue Col Lances Tes (Notes) Aug     Image: Col Lances Tes (Notes) Aug     Image: Col Lances Tes (Notes) Aug       114     DRU Minue Res Processo Des Tes (Notes) Aug     Image: Col Lances Tes (Notes) Aug     Image: Col Lances Tes (Notes) Aug       115     DRU Minue Res Processo Des Tes (Notes) Aug     Image: Col Lances Tes (Notes) Aug     Image: Col Lances Tes (Notes) Aug       115     DRU Minue Res Processo Des Tes (Notes) Aug     Image: Col Lances Tes (Notes) Aug     Image: Col Lances Tes (Notes) Aug       116     DRU Minue Res (Notes) Aug     Tes (Notes) Aug     Image: Col Lances Tes (Notes) Aug     Image: Col Lances Tes (Notes) Aug       117     DRU Minue Res (Notes) Aug     Tes (Notes) Aug     Image: Col Lances Tes (Notes) Aug				
1110     EXAMU ADML Labora's ExaMU ADML LASE Syntax Hys     Image: Control add Labora's The SAMU ADML LASE Syntax Hys       112     EXAMU ADML CALL Labora's The SAMU ADL LASE Syntax Hys     Image: Control add Labora's The SAMU ADML LASE Syntax Hys       112     EXAMU ADML RASE IS ADD Labora's The SAMU ADML Syntax Hys     Image: Control add Labora's The SAMU ADML Syntax Hys       112     EXAMU ADML RASE IS ADD Labora's The SAMU ADML Syntax Hys     Image: Control add Labora's The SAMU ADML Syntax Hys       112     EXAMU ADML RASE IS ADD Labora's The SAMU ADML Syntax Hys     Image: Control add Labora's The SAMU ADML Syntax Hys       112     EXAMU ADML RASE IS ADD Labora's The SAMU ADML Syntax Hys     Image: Control add Labora's The SAMU ADML Syntax Hys       112     EXAMU ADML RASE IS ADD Labora's The SAMU ADML Syntax Hys     Image: Control AdML Hys       113     EXAMU ADML RASE IS ADD Labora's The SAMU ADML Syntax Hys     Image: Control AdML Hys       114     EXAMU ADML RASE IS ADD Labora's The SAMU ADML Syntax Hys     Image: Control AdML Hys       115     EXAMU ADML RASES IS ADD Labora's The SAMU ADML Syntax Hys     Image: Control AdML Hys       116     EXAMU ADML RASES IS ADD Labora's The SAMU ADML Syntax Hys     Image: Control AdML Hys       117     EXAMU ADML RASES IS ADD Labora's The SAMU ADML RASE IS ADD Labora's The SAMU ADML RASE IS ADD Labora's The SAMU ADML RASES IS ADD	714	SDRAM CAS Latencies Supported,Fourth Byte		00
Int     No.     Column       Int     Column     Column       Int<				00
117     IDAM Minima CAL Lawre, The MANNIAL Star Synthesin Pay     IDAM Minima CAL Lawre, The MANNIAL Star Synthesin Pay       117     IDAM Minima ARS to CAL Lawre, The MANNIAL Star Synthesin Pay     IDAM Minima ARS to CAL Lawre, The MANNIAL Synthesin Pay       117     IDAM Minima ARS to CAL Lawre, The MANNIAL Synthesin Pay     IDAM Minima ARS to CAL Lawre, The MANNIAL Synthesin Pay       117     IDAM Minima ARS to CAL Lawre, The MANNIAL Synthesin Pay     IDAM Minima ARS to CAL Lawre, The MANNIAL Synthesin Pay       117     IDAM Minima ARS to CAL Lawre, The MANNIAL Synthesin Pay     IDAM Minima ARS to CAL Lawre, The MANNIAL Synthesin Pay       117     IDAM Minima ARS to CAL Lawre, The MANNIAL Synthesin Pay     IDAM Minima ARS to CAL Lawre, The MANNIAL Synthesin Pay       117     IDAM Minima ARS to CAL Lawre, The MANNIAL Synthesin Pay     IDAM Minima ARS to CAL Lawre, The MANNIAL Synthesin Pay       117     IDAM Minima ARS to CAL Lawre, The MANNIAL Synthesin Pay     IDAM Minima ARS to CAL Lawre, The MANNIAL Synthesin Pay       117     IDAM Minima ARS to CAL Lawre, The MANNIAL Synthesin Pay     IDAM Minima ARS to CAL Lawre, The MANNIAL Synthesin Pay       117     IDAM Minima ARS to CAL Lawre, The MANNIAL Synthesin Pay     IDAM Minima ARS to CAL Lawre, The MANNIAL Synthesin Pay       118     IDAM Minima ARS to CAL Lawre, The MANNIAL Synthesin Pay     IDAM Minima ARS to CAL Lawre, The MANNIAL Synthesin Pay       118     IDAM Minima ARS to CAL Lawre, The MANNIAL Synthesin Pay     IDAM Minima ARS to CAL Lawre, The MANNIAL Synthesin Pay    <				00
III.         DBAM Minue OS Lawor, New Munchash Sprichter Bys         III.           III. BAMA Minue ASIs Loc Daug, Yma SpComiguais Sprichter Bys         III.           III. BAMA Minue ASIs Loc Daug, Yma SpComiguais Sprichter Bys         III.           III. BAMA Minue ASIs Loc Daug, Yma SpComiguais Sprichter Bys         III.           III. BAMA Minue ASIs Loc Daug, Yma SpComiguais Sprichter Bys         III.           III. BAMA Minue Asis Loc Daug, Yma SpComiguais Sprichter Bys         III.           III. BAMA Minue Asis Loc Daug, Yma SpComiguais Sprichter Bys         III.           III. BAMA Minue Asis Loc Daug, Yma SpComiguais Sprichter Bys         III.           III. BAMA Minue Asis Loc Daug, Yma SpComiguais Sprichter Bys         III.           III. BAMA Minue Asis Loc Daug, Yma SpComiguais Sprichter Bys         III.           III. BAMA Minue Asis Loc Daug, Yma SpComiguais Sprichter Bys         III.           III. BAMA Minue Asis Loc Daug, Yma SpComiguais Sprichter Bys         III.           III. BAMA Minue Asis Loc Daug, Yma SpComiguais Sprichter Bys         IIII.           III. BAMA Minue Asis Loc Daug, Yma SpComiguais Sprichter Bys         IIII.           III. BAMA Minue Asis Loc Daug, Yma SpComiguais Sprichter Bys         IIIII.           III. BAMA Minue Asis Loc Daug, Yma SpComiguais Sprichter Bys         IIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII				00
Image: Section of Section of Section Se				00
Tot         EMAM Mining Mike Sol Boys The gROOM (Mod SynChard Pys         Col         Col <td< td=""><td></td><td></td><td></td><td></td></td<>				
T1     DAM Moning Res Processo Days     Control       T2     DAM Moning Res Processo Days     Res Processo Days       T2     DAM Moning Active to Any Streem Monitor Service Page       T2     DAM Moning Active to Any Streem Monitor Service Page       T2     DAM Moning Active to Any Streem Monitor Service Page       T2     DAM Moning Active to Any Streem Monitor Service Page       T2     DAM Moning Active to Any Streem Monitor Service Page       T2     DAM Moning Active to Any Streem Monitor Service Page       T2     DAM Moning Active to Any Streem Monitor Service Page       T2     DAM Moning Page Service Page Service Page       T2     DAM Moning Page Service Page Service Page       T2     DAM Moning Page Service Page Service Page Service Page       T2     DAM Moning Page Service Page Serv				00
T2     SAMU Minima Rev Processo Days The gRPM million Starts Pain     Control       SAMU Minima Adves to Processo Days The gRPM million Starts Pain     Control       SAMU Minima Adves to Processo Days The gRPM million Starts Pain     Control       SAMU Minima Adves to Processo Days The gRPM million Starts Pain     Control       SAMU Minima Adves to Processo Days The gRPM million Starts Pain     Control       SAMU Minima Adves to Processo Days The gRPM million Starts Pain     Control       SAMU Minima Adves to Processo Days The gRPM million Starts Pain     Control       SAMU Minima Adves to Processo Days The gRPM million Starts Pain     Control       SAMU Minima Revers Davas The gRPM million Starts Pain     Control       SAMU Minima Revers Davas The gRPM million Starts Pain     Control       SAMU Minima Revers Davas The gRPM million Starts Pain     Control       SAMU Minima Revers Davas The gRPM million Starts Pain     Control       SAMU Minima Revers Davas The gRPM million Starts Pain     Control       SAMU Minima Revers Davas The gRPM million Starts Pain     Control       SAMU Minima Revers Davas The gRPM million Starts Pain     Control       SAMU Minima Revers Davas The gRPM million Starts Pain     Control       SAMU Minima Revers Davas The gRPM million Starts Pain     Control       SAMU Minima Revers Davas The gRPM million Starts Pain     Control       SAMU Minima Revers Davas The gRPM million Starts Pain     Control </td <td>720</td> <td>SDRAM Minimum RAS to CAS Delay Time (IRCDmin),Most Significant Byte</td> <td></td> <td>00</td>	720	SDRAM Minimum RAS to CAS Delay Time (IRCDmin),Most Significant Byte		00
T2       BAM Minimum Action & Penchage Datar, Time pREAmin Last Eigenstrat Byte       Image: Control of C	721	SDRAM Minimum Row Precharge Delay Time (RPmin).Least Significant Byte		00
12     BAVA Minimum Active Schwarthers BavAmm (Most Big/March Big/Marc	722	SDRAM Minimum Row Precharge Delay Time (IRPmin).Most Significant Byte		00
175     BAVM Minimum Active Markensh Duer, Transflören J. Laust Eigenstrater Byle     Image: Status Active Markensh Duer, Transflören J. Laust Eigenstrater Byle       176     BAVM Minimum Active Markensh Duer, Transflören J. Laust Eigenstrater Byle     Image: Status Active Markensh Duer, Transflören J. Laust Eigenstrater Byle       177     BAVM Minimum Anders Active Markensh Duer, Transflören J. Laust Eigenstrater Byle     Image: Status Active Markensh Duer, Transflören J. Laust Eigenstrater Byle       178     BAVM Minimum Anders Active Markensh Duer, Transflören J. Laust Eigenstrater Byle     Image: Status Active Markensh Duer, Transflören J. Laust Eigenstrater Byle       179     BAVM Minimum Anders Active Markensh Duer, Transflören J. Laust Eigenstrater Byle     Image: Status Active Markensh Duer, Transflören J. Laust Eigenstrater Byle       170     BAVM Minimum Anders Active Markensh Duer, Transflören Deltaser Byle     Image: Status Active Markensh Duer, Transflören Deltaser Byle       171     BAVM Minimum Anders Active Markensh Duer, Transflören Deltaser Byle     Image: Status Active Markensh Duer, Transflören Deltaser Byle       172     BAVM Minimum Anders Active Markensh Duer, Transflören Deltaser Byle     Image: Status Active Markensh Duer, Transflören Deltaser Byle       173     BAVM Minimum Anders Active Markensh Duer, Transflören Deltaser Byle     Image: Status Active Markensh Duer, Transflören Deltaser Byle       174     BAVM Minimum Anders Byle Status Active Markensh Duer, Transflören Deltaser Byle Status Active Markensh Duer, Transflören Deltaser Byle Status Active Markensh Duer, Transflören Deltaser Byle Status Active	723	SDRAM Minimum Active to Precharge Delay Time (IRASmin),Least Significant Byte		00
175     BAVM Minimum Active Markensh Duer, Transflören J. Laust Eigenstrater Byle     Image: Status Active Markensh Duer, Transflören J. Laust Eigenstrater Byle       176     BAVM Minimum Active Markensh Duer, Transflören J. Laust Eigenstrater Byle     Image: Status Active Markensh Duer, Transflören J. Laust Eigenstrater Byle       177     BAVM Minimum Anders Active Markensh Duer, Transflören J. Laust Eigenstrater Byle     Image: Status Active Markensh Duer, Transflören J. Laust Eigenstrater Byle       178     BAVM Minimum Anders Active Markensh Duer, Transflören J. Laust Eigenstrater Byle     Image: Status Active Markensh Duer, Transflören J. Laust Eigenstrater Byle       179     BAVM Minimum Anders Active Markensh Duer, Transflören J. Laust Eigenstrater Byle     Image: Status Active Markensh Duer, Transflören J. Laust Eigenstrater Byle       170     BAVM Minimum Anders Active Markensh Duer, Transflören Deltaser Byle     Image: Status Active Markensh Duer, Transflören Deltaser Byle       171     BAVM Minimum Anders Active Markensh Duer, Transflören Deltaser Byle     Image: Status Active Markensh Duer, Transflören Deltaser Byle       172     BAVM Minimum Anders Active Markensh Duer, Transflören Deltaser Byle     Image: Status Active Markensh Duer, Transflören Deltaser Byle       173     BAVM Minimum Anders Active Markensh Duer, Transflören Deltaser Byle     Image: Status Active Markensh Duer, Transflören Deltaser Byle       174     BAVM Minimum Anders Byle Status Active Markensh Duer, Transflören Deltaser Byle Status Active Markensh Duer, Transflören Deltaser Byle Status Active Markensh Duer, Transflören Deltaser Byle Status Active	724	SDRAM Minimum Active to Precharge Delay Time (RASmin).Most Significant Byte		00
The     DeVM Minimum Active Machene Dury: IntereffCrein J Molt Eigenstrate Type     Image: Control State Stat				00
171     DBAM Minum, Wite Recovery Trans pRMemi (Mail Edge/Carl Byle       172     DBAM Minum, Wite Recovery Trans pRMemi (Mail Edge/Carl Byle       173     DBAM Minum, Relash Recovery Diale, TranspRC::nini_Last Significant Byle       174     DBAM Minum, Relash Recovery Diale, TranspRC::nini_Last Significant Byle       175     DBAM Minum, Relash Recovery Diale, TranspRC::nini_Last Significant Byle       176     DBAM Minum, Relash Recovery Diale, TranspRC::nini_Last Significant Byle       177     DBAM Minum, Relash Recovery Diale, TranspRC::nini_Last Significant Byle       178     DBAM Minum, Relash Recovery Diale, TranspRC::nini_Last Significant Byle       179     DBAM Minum, Relash Recovery Diale, TranspRC::nini_Last Significant Byle       170     DBAM Minum, Relash Recover, Diale, TranspRC::nini_Last Significant Byle       171     DBAM Minum, Relash Recover, Diale, TranspRC::nini_Last Significant Byle       171     DBAM Minum, Colore Relation, Relation, Significant Byle       172     Diale Minut Colore Relation       173     Diale Minut Colore Relation       174     Aylesine GAR Minut       175     Colicial Minut Colore Relation       176     Colicial Minut Colore Relation       177     Diale Colore Relation       178     Colicial Minut Colere Relation       179     Diale Colere Relation       170     Diale Relation       171     Diale Relation </td <td></td> <td></td> <td></td> <td>00</td>				00
1710     DRAM Monum York Recovery The pRVPerior Multi Significant Bys     1       1720     DRAM Monum Relates Recovery Data Transprection Multis Significant Bys     1       1720     DRAM Monum Relates Recovery Data Transprection Multis Significant Bys     1       1720     DRAM Monum Relates Recovery Data Transprection Multis Significant Bys     1       1720     DRAM Monum Relates Recovery Data Transprection Multis Significant Bys     1       1720     DRAM Monum Relates Recovery Data Transprection Multis Significant Bys     1       1721     DRAM Monum Relates Recovery Data Transprection Multis Significant Bys     1       1721     DRAM Monum Relates Recovery Data Transprection Multis Significant Bys     1       1721     DRAM Monum Relates Recovery Data Transprection Multis Significant Bys     1       1721     DRAM Monum Relates Recovery Data Transprection Multis Significant Bys     1       1721     Draviant Relates Recovery Data Transprection Multis Significant Bys     1       1721     Andread Monury Conte Recover Data Significant Bys     1       1721     Andread Monury Conte Recover Data Significant Bys     1       1731     Monu York Bins Box Conte Recover Data Significant Bys     1       1741     Monu York Bins Box Conte Recover Data Significant Bys     1       1741     Monu York Bins Box Conte Recover Data Significant Bys     1       1741     Monu York Bins				00
179     BOM Minum Relate Recovery Datay Treat/PCCInn(Last Significant Ppin       171     BOM Minum Relate Recovery Datay Treat/PCCInn(Last Significant Ppin       171     BOM Minum Relate Recovery Datay Treat/PCCInn(Last Significant Ppin       173     BOM Minum Relate Recovery Datay Treat/PCCInn(Last Significant Ppin       173     BOM Minum Relate Recovery Datay Treat/PCCInn(Last Significant Ppin       174     BOM Minum Relate Recovery Datay Treat/PCCInn(Last Significant Ppin       175     BOM Minum Relate Recovery Datay Treat/PCCInn(Last Significant Ppin       176     Control Minum Relate Recovery Datay Treat/PCCInn(Last Significant Ppin       177     Anoraced Minum Relate Recovery Data Treat/PCCInn(Last Significant Ppin To-Proti)       178     Anoraced Minutery Control (CN) for Base Contigue to Sector, Last Significant Ppin To-Proti)       178     Anoraced Minutery Control (CN) for Base Contigue to Sector, Last Significant Ppin To-Proti)       179     Monitor Minutery Control (CN) for Base Contigue to Sector, Mont Significant Ppin To-Proti)       171     Monitor Minutery Control (CN) for Base Contigue to Sector, Mont Significant Ppin To-Proti)       172     Montory Control (CN) for Base Contigue to Sector, Mont Significant Ppin To-Proti)       173     Montory Control (CN) for Base Control (CN) for Ba				00
100       DRAM Minume Relates Recovery Daily "met#PCC-instrukters Phy       Image: Content Relates Recovery Daily "met#PCC-instrukters Phy         110       DRAM Minume Relates Recovery Daily "met#PCC-instrukters Phy       Image: Content Relates Recovery Daily "met#PCC-instrukters Phy         110       DRAM Minume Relates Recovery Daily "met#PCC-instrukters Phy       Image: Content Relates Recovery Daily "met#PCC-instrukters Phy         111       DRAM Minume Relates Recovery Daily "met#PCC-instrukters Phy       Image: Content Relates Recovery Daily "met#PCC-instrukters Phy         112       DRAM Minume Relates Recovery Daily "met#PCC-instrukters Phy       Image: Content Relates Recovery Daily "met#PCC-instrukters Phy         113       Draws Minimum Relates Recovery Daily "met#PCC-instrukters Phy       Image: Content Relates Recovery Daily The#PCC-instrukters Phy         114       Draws Reference Recovery Daily The#PCC-instrukters Phy       Image: Content Relates Recovery Daily The#PCC-instrukters Phy       Image: Co				
11       DRMM Minume Relates Recovery Delay "met#RCEINILLASES Eginfacet Byte       0         12       DRMM Minume Relates Recovery Delay "met#RCEINILLASES Eginfacet Byte       0         13       DRMM Minume Relates Recovery Delay "met#RCEINILLASES Eginfacet Byte       0         14       DRMM Minume Relates Recovery Delay "met#RCEINILLASES Eginfacet Byte       0         15       DRMM Minume Relates Recovery Delay "met#RCEINILLASES Eginfacet Byte       0         16       Advacced Minume Relates Recovery Delay "met#RCEINILLASES Eginfacet Byte       0         17       DRMM Minume Relates Recovery Delay The#RCEINILLASES Eginfacet Bytem bytes T04-7051       0         17       Ordical Recovery Delay Cherred Minume Relates Science Relation Bytem T04-7051       0         17       Ordical Recovery Delay Cherred Relation Bytem T04-7051       0         17       Delay Minume Check Relation Bytem Science Relation Bytem T04-7051       0         17       Delay Minume Check Relation Bytem Science Relation Bytem T04-7051       0         17       Delay Minume Check Relation Bytem Science Relation Bytem T04       0         17       Delay Minume Check Relation Bytem Science Relatio				00
12       SPAN. Minimum Relikes Recovery Daily "met#RPCLains Market Significant Ryin       Image: Control of Control				00
131       DSMAM Minume Relates Recovery Dairy TransBPCobinitAnd Byrincard Byris       0         141       DSMAM Minume Relates Recovery Dairy TransBPCobinitAnd Byrincard Byris       0         153       Johnson Merine Relates Recovery Dairy TransBPCobinitAnd Byrincard Byris       0         154       Displand Merino Relates Recovery Dairy TransBPCobinitAnd Byrincard Byris       0         154       Displand Merino Relate Recovery Dairy TransBPCobinitAnd Byris       0         154       Displand Merino Relate Recovery Dairy TransBPCobinitAnd Byris       0         155       Vencion Relationary Cost (CPC) To Base Configures on Sector, Loss Significant Byris To-PCO)       0         156       Vencion Relationary Cost (CPC) To Base Configures on Sector, Loss Significant Byris To-PCO)       0         156       Model VDD Voltag Level       0         157       Model VDD Voltag Level       0         158       DERMA Minume Cycis The BCAVCHRINI, VBS ND       0         158       DERMA Minume Cycis The BCAVCHRINI, VBS ND       0         158       DERMA Minume Cycis The BCAVCHRINI, VBS ND       0         158       DERMA Minume Cycis The BCAVCHRINI, VBS ND       0         158       DERMA Minume Cycis The BCAVCHRINI, VBS ND       0         158       DERMA Minume Cycis The BCAVCHRINI, VBS ND       0         158<	731	SDRAM Minimum Refresh Recovery Delay Time(tRPC2min),Least Significant Byte		00
14     EMAM Minume, Relative Root Op Days     0       15     Advanced Memory, One official mathy Relatives     0       16     Advanced Memory, One official mathy Relatives     0       17     Advanced Memory, One official mathy Relatives     0       18     Advanced Memory, One official mathy Relatives     0       19     Version Relatives     0       19     Version Relatives     0       19     Advanced Memory, One official math Relatives for Section, Most off Relatives Torker No.     0       19     Mosta WD Vorsion Level     0       19     Mosta WD Vorsion Level     0       10     Mosta WD Vorsion Level     0       11     Mosta WD Vorsion Level     0       12     Mosta WD Vorsion Level     0       13     SPMAM Minum, Orych The SOLVMERIN Level M     0       14     SPMAM Minum, Orych The SOLVMERIN Level M     0       15     SPMAM Minum, Orych The SOLVMERIN Level M     0       16     SPMAM Minum, Orych The SOLVMERIN Level M     0       17     SOMMA Minum, Orych The SOLVMERIN Level M     0       17     SOMMA Minum, Orych The SOLVMERIN Level M     0       17     SOMMA Minum, Orych The SOLVMERIN Level M     0       17     SOMMA Minum, Orych The SOLVMERIN Level M     0       17 </td <td>732</td> <td>SDRAM Minimum Refresh Recovery Delay Time(RFC2min).Most Significant Byte</td> <td></td> <td>00</td>	732	SDRAM Minimum Refresh Recovery Delay Time(RFC2min).Most Significant Byte		00
19-brd         BYUD must be code at 600         0           19-brd         Advanced Meany Overlection(P makins)         0           19-brd         Code Rate Mode         0           19-brd         Code Stop Code Rate Mode         0           19-brd         Code Stop Code Rate Mode         0           19-brd         Code Stop Code Rate Mode         0           19-brd         Code Rate Mode         0	733	SDRAM Minimum Refresh Recovery Delay Time(RFCsb).Least Significant Byte		00
712-702         SPSUD_mixt be coded as 0x00         0           713         Advanced Merry Oxer/citic/Life Factures         0           714         System CMD Relia Mode         0           715         Vector Markanov Oxer/Citic/Life Factures on Sector, Last Significant Byter TV-F051         0           716         Optical Relia Mode         0           717         Optical Relia Mode         0           718         Advacute VPP Voltage Level         0           719         Moded SVOD Voltage Level         0           710         Moded SVOD Voltage Level         0           711         Moded SVOD Voltage Level         0           718         Relia Marce Vice Structure Significant Byte         0           719         ROMA Marken Cycle These CAVVemin Least Significant Byte         0           710         ROMA Marken Cycle These CAVVemin Least Significant Byte         0           711         ROMA Marken Cycle Life CavVemin Least Significant Byte         0           718         ROMA Marken Cycle Life CavVemin Least Significant Byte         0           719         ROMA CA LiferCole Significant Byte         0         0           710         ROMA CA LiferCole Significant Byte         0         0           7110         ROMA CA LiferCole	734	SDRAM Minimum Refresh Recovery Delay Time(RRCsbmin), Most Significant Byte		00
131     Advanced Memory Oversicoling Factures     0       141     System Cheske Mode     0       152     Versicor Favoranity Biver, HSVD     0       153     Advanced Memory Oxel (RCI) for Bass Confuges Iton Section, Lasst Significant Biver hybes 70-763)     0       157     Opticial Redundery Code (RCI) for Bass Confuges Iton Section, Mast Biotecon Biver hybes 70-763)     0       158     https://dx.Mci and Section Lasst Significant Biver hybes 70-763)     0       159     https://dx.Mci and Section Lasst Significant Biver hybes 70-763)     0       150     Mode YED Virtisga Level     0       150     Mode YED Virtisga Level     0       151     Mode YED Virtisga Level     0       152     Moreon Constrain Year Biver Biotecon Biver     0       153     SIGMA Minimum Cycite Theng Sick/Worein Justa Significant Bive     0       154     SIGMA Minimum Cycite Theng Sick/Worein Justa Significant Bive     0       155     SIGMA CAS Labercele Sizonback/Bive Bive     0     0       156     SIGMA CAS Labercele Sizonback/Bive Bive     0     0       157     SIGMA CAS Labercele Sizonback/Bive Bive     0     0       158     SIGMA Minimum CAS Labercele Bive     0     0       159     SIGMA Minimum CAS Labercele Bive     0     0       150     SIGMA Minimum CAS La	735-762			00
144     system CAD Rate Mode     0       154     Optical Redundary Code (RDT vb Bas Configure Bon Sacton, Last Significant Byter byte 704-765)     0       155     Optical Redundary Code (RDT vb Bas Configure Bon Sacton, Last Significant Byter byte 704-765)     0       158     Andrig Mudaix VbP Vilage Larei     0       159     Mode VD Vilage Larei     0       150     Mode VD Vilage Larei     0       151     Mode VD Vilage Larei     0       152     Mode VD Vilage Larei     0       153     Mode VD Vilage Larei     0       154     SpotM Minnum Cycle The gCAX/Grani, Last Significant Byte     0       155     SpotM Andrean Cycle The gCAX/Grani, Last Significant Byte     0       155     SpotM Andrean Cycle The gCAX/Grani, Last Significant Byte     0       155     SpotM Andrean Cycle The gCAX/Grani, Last Significant Byte     0       155     SpotM Andrean Cycle The gCAX/Grani, Last Significant Byte     0       155     SpotM Andrean Cycle The gCAX/Grani, Last Significant Byte     0       156     SpotM Andrean Significant Byte     0       156     SpotM Andrean Significant Byte     0       156     SpotM Andrean Cycle The gCAX/Grani, Byte Significant Byte     0       156     SpotM Minnum Cycle The gCAX/Grani, Byte Significant Byte     0       156     Spo				00
195     Vector Personality Epis RKV0     0       195     Vector Redundancy Code (SRC) for Base Configures ton Section. Last Singlifount Bught bytes T04-765)     0       197     Operical Redundancy Code (SRC) for Base Configures ton Section. Last Singlifount Bught bytes T04-765)     0       198     Pricial Redundancy Code (SRC) for Base Configures ton Section. Most Sectin. Most Sectin. Most Section. Most Sectio				00
196       Cyclical Rebundsey: Code (SPC) for Base Configure Son Section, Most Significant Physics 704-796).       9         197       Cyclical Rebundsey: Code (SPC) for Base Configure Son Section, Most Significant Physics 704-796).       9         198       Refitial Mundal (MP Villable Level       9         198       Mondal VDO Visiops Level       9         199       Mondal VD Visiops Level       9				00
1717       Cpricial Rebundancy Code (RPL) to Base Configure Son Section, Most Bight Regularing Press 704-761)       0         181       Refuil: A Module VEP Visional Level       0         170       Module VED Visional Level       0         171       Module VED Visional Level       0         172       Module VED Visional Level       0         173       Module VED Visional Level       0         174       Module VED Visional Level       0         175       SPMAM Minimum Cycle Time gCXL/Visini Llasst Significant Byle       0         174       SDFMAM CAS Latencies Signofocal, Rise Byle       0         175       SDFMAM CAS Latencies Signofocal, Shored Byle       0         176       SDFMAM CAS Latencies Signofocal, Shored Byle       0         178       SDFMAM CAS Latencies Signofocal, Shored Byle       0         179       SDFMAM CAS Latencies Signofocal, Shored Byle       0         179       SDFMAM CAS Latencies Signofocal Byle       0         179       SDFMAM CAS Latencies Signofocal Byle       0         170       SDFMAM Minimum CAS Latency Time BA/LiniLlasst Significant Byle       0         179       SDFMAM Minimum RAS By CAS Daily Time BR/DeminiLlasst Significant Byle       0         171       SDFMAM Minimum RAS By CAS Daily Time BR/DeminiLla				
198     Profile 2 Model VP Valage Level     0       196     Model TOV Valage Level     0       171     Model TOV Valage Level     0       172     Model TOV Valage Level     0       173     SDRAM Minimur Cycle Time BCX/CRIENTLY RSVD     0       174     SDRAM Minimur Cycle Time BCX/CRIENTLY RSVD     0       175     SDRAM CAS Labacies Supported.First Byte     0       176     SDRAM CAS Labacies Supported.First Byte     0       177     SDRAM CAS Labacies Supported.First Byte     0       178     SDRAM CAS Labacies Supported.First Byte     0       179     SDRAM CAS Labacies Supported.First Byte     0       179     SDRAM CAS Labacies Supported.First Byte     0       179     SDRAM CAS Labacies Supported.First Byte     0       170     SDRAM CAS Labacies Supported.First Byte     0       171     SDRAM CAS Labacies Supported.First Byte     0       172     SDRAM Minimur CAS Labacies Supported.First Byte     0       173     SDRAM Minimur CAS Labacies Supported.First Byte     0       174     SDRAM Minimur CAS Labacies Supported.First Byte     0       175     SDRAM Minimur CAS Labacies Supported.First Byte     0       174     SDRAM Minimur CAS Labacies Supported.First Byte     0       175     SDRAM Minimur CAS Labacie				00
199     Module VDD Vistage Level     0       770     Module VDD Vistage Level     0       771     Module VDD Vistage Level     0       772     Module VDD Vistage Level     0       773     SPEAM Minimum Cycic Time RCXVCRimin_Least BiginEcart Byte     0       774     SDEAM Minimum Cycic Time RCXVCRimin_Least BiginEcart Byte     0       775     SDEAM CAS Latencies Supported.Filter Byte     0       776     SDEAM CAS Latencies Supported.Filter Byte     0       777     SDEAM CAS Latencies Supported.Filter Byte     0       778     SDEAM CAS Latencies Supported.Filter Byte     0       778     SDEAM CAS Latencies Supported.Filter Byte     0       778     SDEAM CAS Latencies Supported.Filter Byte     0       779     SDEAM CAS Latencies Supported.Filter Byte     0       778     SDEAM Minimum CAS Latencies Supported.Filter Byte     0       779     SDEAM Minimum CAS Latencies Supported.Filter Byte     0       778     SDEAM Minimum CAS Latencies Supported.Filter Byte     0       779     SDEAM Minimum CAS Latencies Supported.Filter Byte     0       778     SDEAM Minimum CAS Latencies Supported.Filter Byte     0       778     SDEAM Minimum CAS Latencies Time RASIMINIAL Byte     0       778     SDEAM Minimum CAS Latencies Time RASIMINIAL Byte     0	767			00
170     Module VDCOV Voltage Level     0       171     Module VD Voltage Level     0       172     Memory Controller Voltage Level     0       173     BDRAM Minimum Cycles Time (DCAVVenin).Lasst Significant Byte     0       174     BDRAM Minimum Cycles Time (DCAVVenin).Lasst Significant Byte     0       175     BDRAM Advinum Cycles Time (DCAVVenin).Most Significant Byte     0       176     BDRAM Advinum Cycles Time (DCAVVenin).Most Significant Byte     0       177     BDRAM Advinum Cycles Time (DCAVVenin).Most Significant Byte     0       178     BDRAM Advinum CASL Latencies Supported.Florth Byte     0       178     BDRAM Advinum CASL Latencies Supported.Florth Byte     0       178     BDRAM Minimum CASL Latencies Supported.Florth Byte     0       179     BDRAM Minimum CASL Latencies Supported.Florth Byte     0       171     BDRAM Minimum CASL Latencies Time (BCDMin).Last Significant Byte     0       171     BDRAM Minimum CASL Latencies Time (BCDMin).Last Significant Byte     0       171     BDRAM Minimum CASL Latencies Time (BCDMin).Last Significant Byte     0       172     BDRAM Minimum CASL Significant Byte     0       173     BDRAM Minimum CASL Significant Byte     0       174     BDRAM Minimum CASL Significant Byte     0       175     BDRAM Minimum Cycles Datay Time (BRCAmin	768	Profile2 :Module VPP Voltage Level		00
171     Modula TBD Voltage Level - PHSI SYTIES CURRENTLY REVD     Immory Control PhSI Sytem 15 CURRENTLY REVD       172     Memory Control PhSI Sytem 15 CURRENTLY REVD     Immory Control PhSI Sytem 15 CURRENTLY REVD       173     SDRAM Minimur Cycls Time (CAVVGmin) Most Significant Byte     Immory Control PhSI System 15 CURRENTLY REVD       174     SDRAM Minimur Cycls Time (CAVVGmin) Most Significant Byte     Immory Control PhSI System 15 CURRENTLY REVD       175     SDRAM Additionur Cycls Time (CAVVGmin) Most Significant Byte     Immory Control PhSI System 15 CURRENTLY REVD       175     SDRAM Additionur CAS Laterice Supporter, Fund Byte     Immory Control PhSI Significant Byte       176     SDRAM Additionur CAS Laterice Supporter, Fund Byte     Immory Control PhSI Significant Byte       178     SDRAM Minimur CAS Laterice Supporter, Fund Byte     Immory CAS Laterice Significant Byte       178     SDRAM Minimur CAS Laterice Time (SCDmin) Most Significant Byte     Immory CAS Laterice Significant Byte       178     SDRAM Minimur Active to Dischin Time (SRCDmin) Most Significant Byte     Immory CAS Laterice Significant Byte       178     SDRAM Minimur Active to Dischin Time (SRCDmin) Most Significant Byte     Immory CAS Laterice Significant Byte       179     SDRAM Minimur Active to Disching Bask Significant Byte     Immory CAS Laterice Significant Byte       179     SDRAM Minimur Active to Active Return Disk Time (SRCDmin) Most Significant Byte     Immory Case Laterice Significant Byte	769	Module VDD Voltage Level		00
1772     Marciny Control of Viction Tune (BXAN/Gmin LLaast Bignificant Byta     1       1773     SDRAM Minimum Cycle Time (BXAN/Gmin LLaast Bignificant Byta     1       1774     SDRAM A Minimum Cycle Time (BXAN/Gmin LLaast Bignificant Byta     1       1775     SDRAM A CS Latercice Supported, First Byta     1       1776     SDRAM CAS Latercice Supported, First Byta     1       1776     SDRAM CAS Latercice Supported, First Byta     1       1778     SDRAM CAS Latercice Supported, First Byta     1       178     SDRAM CAS Latercice Supported, First Byta     1       179     SDRAM CAS Latercice Supported, First Byta     1       179     SDRAM Minimum CAS Latercy Time (AAmin LLaast Bignificant Byta     1       178     SDRAM Minimum CAS Latercy Time (AAmin LLaast Bignificant Byta     1       178     SDRAM Minimum CAS Latercy Time (AAmin LLaast Bignificant Byta     1       178     SDRAM Minimum RAS LATERCY Time (AAmin LLaast Bignificant Byta     1       179     SDRAM Minimum RAS Latercy Time (AAmin LLaast Significant Byta     1       178     SDRAM Minimum RAS LATERCY Time (AAmin Laast Significant Byta     1       179     SDRAM Minimum RAS LATERCY Time (AAmin Laast Significant Byta     1       179     SDRAM Minimum RAS LATERCY Time (AAmin Laast Significant Byta     1       179     SDRAM Minimum RASta CAS Delay Time (RRAMin MINASI	770	Module VDDQ Voltage Level		00
773       SCRAM Minimum Cycle Time (CXAVCenin),Last Significant Byle       0         774       SCRAM CAS Latercicles Supported,Fint Byle       0         775       SCRAM CAS Latercicles Supported,Fint Byle       0         776       SCRAM CAS Latercicles Supported,Fint Byle       0         778       SCRAM CAS Latercicles Supported,Fint Byle       0         779       SCRAM CAS Latercicles Supported, Fint Byle       0         778       SCRAM Minimum CAS Latercicles Supported, Time Byle       0         778       SCRAM Minimum CAS Latercicles Supported, Time Byle       0         778       SCRAM Minimum CAS Latercicles Supported, Time Byle       0         778       SCRAM Minimum CAS Latercicle Supported, Time Byle       0         778       SCRAM Minimum CAS Latercicle Supported, Time Byle       0         778       SCRAM Minimum As by CAS Dalay Time Byle       0         778       SCRAM Minimum As by CAS Dalay Time Byle       0         778       SCRAM Minimum As byle CAS Dalay Tim	771	Module TBD Voltage Level - THIS BYTE IS CURRENTLY RSVD		00
773       SCRAM Minimum Cycle Time (CXAVCenin),Last Significant Byle       0         774       SCRAM CAS Latercicles Supported,Fint Byle       0         775       SCRAM CAS Latercicles Supported,Fint Byle       0         776       SCRAM CAS Latercicles Supported,Fint Byle       0         778       SCRAM CAS Latercicles Supported,Fint Byle       0         779       SCRAM CAS Latercicles Supported, Fint Byle       0         778       SCRAM Minimum CAS Latercicles Supported, Time Byle       0         778       SCRAM Minimum CAS Latercicles Supported, Time Byle       0         778       SCRAM Minimum CAS Latercicles Supported, Time Byle       0         778       SCRAM Minimum CAS Latercicle Supported, Time Byle       0         778       SCRAM Minimum CAS Latercicle Supported, Time Byle       0         778       SCRAM Minimum As by CAS Dalay Time Byle       0         778       SCRAM Minimum As by CAS Dalay Time Byle       0         778       SCRAM Minimum As byle CAS Dalay Tim	772	Memory Controller Voltage Level		00
1774         SCRAM Minimum Cycle Time (CX/VX0ein)/Most Significant Byte         1         1           1755         SCRAM CAS Latercies Supported, Second Byte         1         1           1765         SCRAM CAS Latercies Supported, Second Byte         1         1           1777         SCRAM CAS Latercies Supported, Fuenty Byte         1				00
1775     SCRAM CAS Latencies Supported, Fixie Byte        776     SDRAM CAS Latencies Supported, Fixie Byte        777     SDRAM CAS Latencies Supported, Fixie Byte        778     SDRAM CAS Latencies Supported, Fixie Byte        778     SDRAM CAS Latencies Supported, Fixie Byte        779     SDRAM CAS Latencies Supported, Fixie Byte        780     SDRAM CAS Latencies Supported, Fixie Byte        781     SDRAM Minimum CAS Latency Time (MAmin)Latest Significant Byte        782     SDRAM Minimum CAS Latency Time (MAmin)Latest Significant Byte        783     SDRAM Minimum CAS Latency Time (MAmin)Latest Significant Byte        784     SDRAM Minimum RAS to CAS Dalay Time (RPEmin)Latest Significant Byte        785     SDRAM Minimum RAS to CAS Dalay Time (RPEmin)Latest Significant Byte        786     SDRAM Minimum Row Precharge Dalay Time (RPEmin)Latest Significant Byte        787     SDRAM Minimum Active to Precharge Dalay Time (RPEmin)Latest Significant Byte        788     SDRAM Minimum Active to Precharge Dalay Time (RPEmin)Latest Significant Byte        789     SDRAM Minimum Active to Active/Refersh Dalay Time(RPEmin)Latest Significant Byte        791     SDRAM Minimum Active to Active/Refersh Dalay Time(RPEmin)Latest Significant Byte        793     SDRAM				00
1716     SCRAM CAS Latancies Supported.Second Byte     -     C       1777     SCRAM CAS Latancies Supported.Furth Byte     -     C       178     SCRAM Minimum CAS Latancy Time (MArrin)Least Significant Byte     -     C       178     SCRAM Minimum CAS Latancy Time (MArrin)Least Significant Byte     -     C       178     SCRAM Minimum CAS Latancy Time (MArrin)Least Significant Byte     -     C       178     SCRAM Minimum RAS to CAS Dalay Time (RCDmin)Least Significant Byte     -     C       178     SCRAM Minimum Row Precharge Dalay Time (RPS-min)Least Significant Byte     -     C       178     SCRAM Minimum Active to Precharge Dalay Time (RPS-min)Least Significant Byte     -     C       178     SCRAM Minimum Active to Precharge Dalay Time (RPS-min)Least Significant Byte     -     C       179     SCRAM Minimum Active to Active Refers Dalay Time (RPS-min)Least Significant Byte     -     C       179     SCRAM Minimum Active to Active Refers Dalay Time(RPC-min)Least Significant Byte     -     C       179     SCRAM Minimum Active to Active Refers Dalay Time(RPC-min)Least Significant Byte     C     C				00
177     SDRAM CAS Latencies Supported.Third Byte     .       778     SDRAM CAS Latencies Supported.Third Byte     .       778     SDRAM CAS Latencies Supported.Third Byte     .       780     SDRAM CAS Latencies Supported.Third Byte     .       780     SDRAM CAS Latencies Supported.Third Byte     .       781     SDRAM Minimum CAS Latency Time (MAmin)Last Significant Byte     .       782     SDRAM Minimum RAS to CAS Delay Time (RCDmin)Last Significant Byte     .       783     SDRAM Minimum RAS to CAS Delay Time (RPCDmin)Last Significant Byte     .       784     SDRAM Minimum RAS to CAS Delay Time (RPCDmin)Last Significant Byte     .       785     SDRAM Minimum Rov Precharge Delay Time (RPCDmin)Last Significant Byte     .       786     SDRAM Minimum Active to Precharge Delay Time (RPCDmin)Last Significant Byte     .       787     SDRAM Minimum Active to Precharge Delay Time (RPCDmin). Last Significant Byte     .       788     SDRAM Minimum Active to Precharge Delay Time (RPCDmin). Last Significant Byte     .       789     SDRAM Minimum Active to Precharge Delay Time (RPCDmin). Last Significant Byte     .       790     SDRAM Minimum Active to Active/Referent Datast Significant Byte     .       791     SDRAM Minimum Referen Recovery Time (RPCImin). Last Significant Byte     .       792     SDRAM Minimum Referen Recovery Time (RPCImin). Most Significant Byte				
178     SDRAM CAS Latencies Supported, Fun Byte     -     0       779     SDRAM CAS Latencies Supported, Fun Byte     -     0       779     SDRAM MCAS Latencies Supported, Fun Byte     -     0       781     SDRAM Minimum CAS Latency Time (MAmin), Most Significant Byte     -     0       782     SDRAM Minimum CAS Latency Time (MAmin), Most Significant Byte     -     0       783     SDRAM Minimum CAS Latency Time (MACINI), Most Significant Byte     -     0       784     SDRAM Minimum RAS to CAS Delay Time (RCDmin), Last Significant Byte     -     0       785     SDRAM Minimum RAVe Procharge Delay Time (RCDmin), Last Significant Byte     -     0       785     SDRAM Minimum Activ to Pincharge Delay Time (RCDmin), Last Significant Byte     -     0       785     SDRAM Minimum Activ to Pincharge Delay Time (RCDmin), Last Significant Byte     -     0       785     SDRAM Minimum Activ to Pincharge Delay Time (RCDmin), Last Significant Byte     -     0       786     SDRAM Minimum Activ to Anctiva/Refresh Delay Time(RCDmin), Last Significant Byte     -     0       796     SDRAM Minimum Activ to Anctiva/Refresh Delay Time(RCDmin), Most Significant Byte     -     0       797     SDRAM Minimum Refresh Recovery Diay Time(RCDmin), Most Significant Byte     -     0       798     SDRAM Minimum Refresh Recovery Diay Time(RCDmin), Mo				00
779     SDRAM CAS Latencies Supported, Fith Byte     -       780     RSVD for future CAS Latency     C       781     SDRAM Minimum CAS Latency Time (MAmin)Last Significant Byte     C       782     SDRAM Minimum CAS Latency Time (MAmin)Last Significant Byte     C       783     SDRAM Minimum RAS to CAS Delay Time (RCDmin)Last Significant Byte     C       784     SDRAM Minimum RAS to CAS Delay Time (RCDmin)Last Significant Byte     C       785     SDRAM Minimum RAS to CAS Delay Time (RCDmin)Last Significant Byte     C       786     SDRAM Minimum Row Precharge Delay Time (RCDmin)Last Significant Byte     C       787     SDRAM Minimum Row Precharge Delay Time (RCDmin)Last Significant Byte     C       788     SDRAM Minimum Active to Precharge Delay Time (RCDmin)Last Significant Byte     C       788     SDRAM Minimum Active to Precharge Delay Time (RCDmin)Last Significant Byte     C       791     SDRAM Minimum Active to Active-Rinken Delay Time(RCDmin)Last Significant Byte     C       791     SDRAM Minimum Active to Active-Rinken Delay Time(RCDmin)Last Significant Byte     C       792     SDRAM Minimum Mitte Recovery Time (WRMin)Last Significant Byte     C       793     SDRAM Minimum Rinken Recovery Delay Time(RPCDrini)Last Significant Byte     C       794     SDRAM Minimum Rinken Recovery Delay Time(RPCDrini)Last Significant Byte     C       795     SDRAM Minimum			•	00
780       RSVD for future CAS Latency       Image: CAS Latency image: (AAmin)Lasst Significant Byte         781       SDRAM Minimum CAS Latency Time (MAmin)Lasst Significant Byte       Image: CAS Data         783       SDRAM Minimum CAS Latency Time (RCDmin)Least Significant Byte       Image: CAS Data         784       SDRAM Minimum RAS to CAS Data       Significant Byte       Image: CAS Data         785       SDRAM Minimum RAP recharge Data       Significant Byte       Image: CAS Data       Image: CAS Data         785       SDRAM Minimum RAP recharge Data       Significant Byte       Image: CAS Data       Im	778	SDRAM CAS Latencies Supported, Fourth Byte	-	00
781       SDRAM Minimum CAS Latency Time (MAmin).Least Significant Byte       0         782       SDRAM Minimum CAS Latency Time (RAmin).Least Significant Byte       0         784       SDRAM Minimum RAS to CAS Delay Time (RCDmin).Most Significant Byte       0         785       SDRAM Minimum RAS to CAS Delay Time (RCDmin).Most Significant Byte       0         786       SDRAM Minimum Row Pricharge Delay Time (RCDmin).Most Significant Byte       0         787       SDRAM Minimum Active to Precharge Delay Time (RASmin).Least Significant Byte       0         788       SDRAM Minimum Active to Precharge Delay Time (RASmin).Least Significant Byte       0         789       SDRAM Minimum Active to Precharge Delay Time (RASmin).Least Significant Byte       0         789       SDRAM Minimum Active to ActiveRatesh Delay Time(RASmin).Most Significant Byte       0         789       SDRAM Minimum Mitte Recovery Time (WRmin).Least Significant Byte       0         791       SDRAM Minimum Mitte Recovery Time (WRmin).Least Significant Byte       0         792       SDRAM Minimum Ratesh Recovery Diay Time(RCFIni).Least Significant Byte       0         793       SDRAM Minimum Ratesh Recovery Diay Time(RFCEIni).Least Significant Byte       0         794       SDRAM Minimum Ratesh Recovery Diay Time(RFCEIni).Most Significant Byte       0         795       SDRAM Minimum Ratesh Recovery Diay	779	SDRAM CAS Latencies Supported, Fifth Byte		00
782       SDRAM Minimum CAS Latency Time (RADmin).Least Significant Byte       0         783       SDRAM Minimum RAS to CAS Delay Time (REDmin).Least Significant Byte       0         784       SDRAM Minimum RAS to CAS Delay Time (REDmin).Least Significant Byte       0         785       SDRAM Minimum Row Precharge Delay Time (REPmin).Least Significant Byte       0         786       SDRAM Minimum Active to Precharge Delay Time (RESmin).Least Significant Byte       0         787       SDRAM Minimum Active to Precharge Delay Time (RESmin).Least Significant Byte       0         788       SDRAM Minimum Active to Active Resonant Delay Time (RESmin).Least Significant Byte       0         789       SDRAM Minimum Active to Active/Refresh Delay Time (RESmin).Most Significant Byte       0         790       SDRAM Minimum Active to Active/Refresh Delay Time (RESmin).Most Significant Byte       0         791       SDRAM Minimum Write Recovery Time (WRMIN).Most Significant Byte       0         793       SDRAM Minimum Refresh Recovery Delay Time(RRPCTimin).Least Significant Byte       0         794       SDRAM Minimum Refresh Recovery Delay Time(RRPCTimin).Least Significant Byte       0         795       SDRAM Minimum Refresh Recovery Delay Time(RRPCTimin).Least Significant Byte       0         795       SDRAM Minimum Refresh Recovery Delay Time(RRPCTimin).Least Significant Byte       0 <t< td=""><td>780</td><td>RSVD for future CAS Latency</td><td></td><td>00</td></t<>	780	RSVD for future CAS Latency		00
783       SDRAM Minimum RAS to CAS Delay Time (RCDmin)Least Significant Byte       0         784       SDRAM Minimum RAS to CAS Delay Time (RCDmin)Least Significant Byte       0         785       SDRAM Minimum Row Precharge Delay Time (RASmin)Least Significant Byte       0         786       SDRAM Minimum Active to Precharge Delay Time (RASmin)Least Significant Byte       0         787       SDRAM Minimum Active to Precharge Delay Time (RASmin)Least Significant Byte       0         788       SDRAM Minimum Active to Precharge Delay Time (RASmin)Least Significant Byte       0         789       SDRAM Minimum Active to Active/Refresh Delay Time (RASmin)Least Significant Byte       0         790       SDRAM Minimum Active to Active/Refresh Delay Time(RASmin)Least Significant Byte       0         791       SDRAM Minimum Write Recovery Time (WRRIM)Least Significant Byte       0         792       SDRAM Minimum Write Recovery Delay Time(RASTmin)Least Significant Byte       0         793       SDRAM Minimum Refresh Recovery Delay Time(RASTmin)Least Significant Byte       0         794       SDRAM Minimum Refresh Recovery Delay Time(RASTmin)Least Significant Byte       0         795       SDRAM Minimum Refresh Recovery Delay Time(RASTmin)Least Significant Byte       0         796       SDRAM Minimum Refresh Recovery Delay Time(RASTmin)Least Significant Byte       0         797	781	SDRAM Minimum CAS Latency Time (AAmin),Least Significant Byte		00
783       SDRAM Minimum RAS to CAS Delay Time (RCDmin)Least Significant Byte       0         784       SDRAM Minimum RAS to CAS Delay Time (RCDmin)Least Significant Byte       0         785       SDRAM Minimum Row Prechargo Delay Time (RASIMI)Least Significant Byte       0         786       SDRAM Minimum Row Prechargo Delay Time (RASIMI)Least Significant Byte       0         787       SDRAM Minimum Active to Prechargo Delay Time (RASIMI)Least Significant Byte       0         788       SDRAM Minimum Active to Prechargo Delay Time (RASIMI)Most Significant Byte       0         789       SDRAM Minimum Active to ActiveRatesh Delay Time (RASIMI).Most Significant Byte       0         790       SDRAM Minimum Mink Recovery Time (WRIMI).Most Significant Byte       0         791       SDRAM Minimum Mink Recovery Time (WRIMI).Most Significant Byte       0         793       SDRAM Minimum Mink Recovery Delay Time(RECTIMIN).Asst Significant Byte       0         794       SDRAM Minimum Refesh Recovery Delay Time(RECTIMIN).Asst Significant Byte       0         795       SDRAM Minimum Refesh Recovery Delay Time(RECTIMIN).Asst Significant Byte       0         795       SDRAM Minimum Refesh Recovery Delay Time(RECTIMIN).Asst Significant Byte       0         796       SDRAM Minimum Refesh Recovery Delay Time(RECTIMIN).Asst Significant Byte       0         797       SDRAM Minimum Refesh Re	782	SDRAM Minimum CAS Latency Time (tAAmin),Most Significant Byte		00
784       SDRAM Minimum RAS to CAS Delay Time (RRCDmin).Most Significant Byte				00
SDRAM Minimum Row Precharge Delay Time (RPmin)Least Significant Byte       1000000000000000000000000000000000000				00
786       SDRAM Minimum Row Procharge Delay Time (RPEmin),Most Significant Byte       100         787       SDRAM Minimum Active to Procharge Delay Time (RASmin),Least Significant Byte       100         788       SDRAM Minimum Active to Procharge Delay Time (RASmin),Least Significant Byte       100         789       SDRAM Minimum Active to Active/Refresh Delay Time (RASmin),Least Significant Byte       100         790       SDRAM Minimum Mettre tacovery Time (WRmin),Least Significant Byte       100         791       SDRAM Minimum Write Racovery Time (WRmin),Least Significant Byte       100         793       SDRAM Minimum Write Racovery Time (WRmin),Most Significant Byte       100         794       SDRAM Minimum Refresh Racovery Delay Time(RFC1min),Least Significant Byte       100         795       SDRAM Minimum Refresh Racovery Delay Time(RFC2min),Least Significant Byte       100         795       SDRAM Minimum Refresh Racovery Delay Time(RFC2min),Most Significant Byte       100         796       SDRAM Minimum Refresh Racovery Delay Time(RFC2min),Most Significant Byte       100         797       SDRAM Minimum Refresh Racovery Delay Time(RFC2min),Most Significant Byte       100         798       SDRAM Minimum Refresh Racovery Delay Time(RFC2min),Most Significant Byte       100         799       SDRAM Minimum Refresh Racovery Delay Time(RFC2min),Most Significant Byte       100				00
787       SDRAM Minimum Active to Precharge Delay Time (RASmin).Least Significant Byte       1000000000000000000000000000000000000				00
788       SDRAM Minimum Active to Precharge Delay Time (RASmin).Most Significant Byte       100         789       SDRAM Minimum Active to Active Refresh Delay Time (RCmin). Least Significant Byte       100         790       SDRAM Minimum Active to Active Refresh Delay Time (RCmin). Least Significant Byte       100         791       SDRAM Minimum Active to Active Refresh Delay Time (RCmin). Most Significant Byte       100         791       SDRAM Minimum Write Recovery Time (WRmin).Most Significant Byte       100         792       SDRAM Minimum Refresh Recovery Delay Time (RFCTIMIN).Most Significant Byte       100         793       SDRAM Minimum Refresh Recovery Delay Time (RFCTIMIN).Most Significant Byte       100         794       SDRAM Minimum Refresh Recovery Delay Time (RFCTIMIN).Most Significant Byte       100         795       SDRAM Minimum Refresh Recovery Delay Time (RFCCIMIN).Most Significant Byte       100         796       SDRAM Minimum Refresh Recovery Delay Time (RFCCIMIN).Most Significant Byte       100         797       SDRAM Minimum Refresh Recovery Delay Time (RFCCIMIN).Most Significant Byte       100         798       SDRAM Minimum Refresh Recovery Delay Time (RFCCIMIN).Most Significant Byte       100         798       SDRAM Minimum Refresh Recovery Delay Time (RFCCIMIN).Most Significant Byte       100         798       SDRAM Minimum Refresh Recovery Delay Time (RFCCIMIN).Most Significant Byte<				
789       SDRAM Minimum Active to Active/Refresh Delay Time(RCmin) Least Significant Byte       100         790       SDRAM Minimum Active to Active/Refresh Delay Time(RCmin) Least Significant Byte       100         791       SDRAM Minimum Write Recovery Time (WRmin) Least Significant Byte       100         792       SDRAM Minimum Write Recovery Delay Time(RFCCmin) Least Significant Byte       100         793       SDRAM Minimum Refresh Recovery Delay Time(RFCCmin) Least Significant Byte       100         794       SDRAM Minimum Refresh Recovery Delay Time(RFCCmin) Least Significant Byte       100         795       SDRAM Minimum Refresh Recovery Delay Time(RFCCImin) Least Significant Byte       100         796       SDRAM Minimum Refresh Recovery Delay Time(RFCCImin) Least Significant Byte       100         797       SDRAM Minimum Refresh Recovery Delay Time(RFCCImin) Most Significant Byte       100         797       SDRAM Minimum Refresh Recovery Delay Time(RFCCImin) Most Significant Byte       100         798       SDRAM Minimum Refresh Recovery Delay Time(RFCCImin) Most Significant Byte       100         798       SDRAM Minimum Refresh Recovery Delay Time(RFCCImin) Most Significant Byte       100         798       SDRAM Minimum Refresh Recovery Delay Time(RFCCImin) Most Significant Byte       100         799       SDRAM Minimum Refresh Recovery Delay Time(RFCCImin) Most Significant Byte       100 <td></td> <td></td> <td></td> <td>00</td>				00
790       SDRAM Minimum Active to Active/Refresh Delay Time(RRCmin) Most Significant Byte       000000000000000000000000000000000000				00
791       SDRAM Minimum Write Recovery Time (WRmin) Least Significant Byte       0         792       SDRAM Minimum Write Recovery Time (WRmin) Most Significant Byte       0         793       SDRAM Minimum Refresh Recovery Delay Time(RFCTImin) Least Significant Byte       0         794       SDRAM Minimum Refresh Recovery Delay Time(RFCTImin) Least Significant Byte       0         795       SDRAM Minimum Refresh Recovery Delay Time(RFCTImin) Least Significant Byte       0         796       SDRAM Minimum Refresh Recovery Delay Time(RFCCImin) Most Significant Byte       0         797       SDRAM Minimum Refresh Recovery Delay Time(RFCCImin) Most Significant Byte       0         798       SDRAM Minimum Refresh Recovery Delay Time(RFCCImin) Most Significant Byte       0         799       SDRAM Minimum Refresh Recovery Delay Time(RFCCImin) Most Significant Byte       0         799       SDRAM Minimum Refresh Recovery Delay Time(RFCCImin) Most Significant Byte       0         798       SDRAM Minimum Refresh Recovery Delay Time(RFCCImin) Most Significant Byte       0         799       SDRAM Minimum Refresh Recovery Delay Time(RFCCImin) Most Significant Byte       0         799       SDRAM Minimum Refresh Recovery Delay Time(RFCCImin) Most Significant Byte       0         799       SDRAM Minimum Refresh Recovery Delay Time(RFCCImin) Most Significant Byte       0         799	789	SDRAM Minimum Active to Active/Refresh Delay Time(tRCmin) Least Significant Byte		00
792       SDRAM Minimum Witte Recovery Time (WRmin) Most Significant Byte       100         793       SDRAM Minimum Refresh Recovery Delay Time(RFC1min) Least Significant Byte       100         794       SDRAM Minimum Refresh Recovery Delay Time(RFC1min) Most Significant Byte       100         795       SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte       100         795       SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte       100         796       SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte       100         797       SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte       100         798       SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte       100         798       SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte       100         798       SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte       100         798       SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte       100         798       SDRAM Memory Overclocking Features       100         827       Advanced Memory Overclocking Features       100         828       System CMD Rate Mode       100       100         829       Vendor Personality Byte - RSVD       100       100	790	SDRAM Minimum Active to Active/Refresh Delay Time(IRCmin) ,Most Significant Byte		00
793       SDRAM Minimum Refresh Recovery Delay Time(RFC1min).Least Significant Byte       100         794       SDRAM Minimum Refresh Recovery Delay Time(RFC2min).Least Significant Byte       100         795       SDRAM Minimum Refresh Recovery Delay Time(RFC2min).Least Significant Byte       100         796       SDRAM Minimum Refresh Recovery Delay Time(RFC2min).Least Significant Byte       100         797       SDRAM Minimum Refresh Recovery Delay Time(RFC2min).Most Significant Byte       100         798       SDRAM Minimum Refresh Recovery Delay Time(RFC2bi.Least Significant Byte       100         798       SDRAM Minimum Refresh Recovery Delay Time(RFC2bi.Least Significant Byte       100         798       SDRAM Minimum Refresh Recovery Delay Time(RFC2binin).Most Significant Byte       100         798       SDRAM Minimum Refresh Recovery Delay Time(RFC2bi.Least Significant Byte       100         799       SDRAM Minimum Refresh Recovery Delay Time(RFC2bi.Least Significant Byte       100         799       SDRAM Monor       100       100         799       SDRAM Memory Overclocking Features       100         827       Advanced Memory Overclocking Features       100         828       System CMD Ret Mode       100       100         829       Vendor Personality Byte - RSVD       100       100         830	791	SDRAM Minimum Write Recovery Time (WRmin).Least Significant Byte		00
794       SDRAM Minimum Refresh Recovery Delay Time(RFC2min).Most Significant Byte       0         795       SDRAM Minimum Refresh Recovery Delay Time(RFC2min).Least Significant Byte       0         796       SDRAM Minimum Refresh Recovery Delay Time(RFC2min).Most Significant Byte       0         797       SDRAM Minimum Refresh Recovery Delay Time(RFC2bin).Most Significant Byte       0         798       SDRAM Minimum Refresh Recovery Delay Time(RFC2bin).Most Significant Byte       0         798       SDRAM Minimum Refresh Recovery Delay Time(RFC2bin).Most Significant Byte       0         798       SDRAM Minimum Refresh Recovery Delay Time(RFC2bin).Most Significant Byte       0         798       SDRAM Minimum Refresh Recovery Delay Time(RFC2bin).Most Significant Byte       0         799426       RSVD,must be coded as 0x00       0         827       Advanced Memory Overclocking Features       0         828       System CMD Rate Mode       0       0         829       Vendor Personality Byte - RSVD       0       0         830       Ovelical Redundancy Code (CRC) for Base Configura tion Section, Least Significant Byte/or bytes 768–829)       0       0	792	SDRAM Minimum Write Recovery Time (tWRmin).Most Significant Byte		00
794       SDRAM Minimum Refresh Recovery Delay Time(RFC2min).Most Significant Byte       0         795       SDRAM Minimum Refresh Recovery Delay Time(RFC2min).Least Significant Byte       0         796       SDRAM Minimum Refresh Recovery Delay Time(RFC2min).Most Significant Byte       0         797       SDRAM Minimum Refresh Recovery Delay Time(RFC2bin).Most Significant Byte       0         798       SDRAM Minimum Refresh Recovery Delay Time(RFC2bin).Most Significant Byte       0         798       SDRAM Minimum Refresh Recovery Delay Time(RFC2bin).Most Significant Byte       0         798       SDRAM Minimum Refresh Recovery Delay Time(RFC2bin).Most Significant Byte       0         798       SDRAM Minimum Refresh Recovery Delay Time(RFC2bin).Most Significant Byte       0         799426       RSVD,must be coded as 0x00       0         827       Advanced Memory Overclocking Features       0         828       System CMD Rate Mode       0       0         829       Vendor Personality Byte - RSVD       0       0         830       Ovelical Redundancy Code (CRC) for Base Configura tion Section, Least Significant Byte/or bytes 768–829)       0       0	793	SDRAM Minimum Refresh Recovery Delay Time(IRFC1min)Least Significant Byte		00
795       SDRAM Minimum Refresh Recovery Delay Time(RFC2min).Least Significant Byte       0         796       SDRAM Minimum Refresh Recovery Delay Time(RFC2min).Most Significant Byte       0         797       SDRAM Minimum Refresh Recovery Delay Time(RFC2min).Most Significant Byte       0         798       SDRAM Minimum Refresh Recovery Delay Time(RFC2b).Least Significant Byte       0         798       SDRAM Minimum Refresh Recovery Delay Time(RFC2b).Least Significant Byte       0         798       SDRAM Minimum Refresh Recovery Delay Time(RFC2b).Least Significant Byte       0         798-82       RSVD,must be coded as 0x00       0         827       Advanced Memory Overclocking Features       0         828       System CMD Rate Mode       0         829       Vendor Personality Byte - RSVD       0         830       Cyclical Redundancy Code (CRC) for Base Configura tion Section, Least Significant Byte(r bytes 768-829)       0				00
796       SDRAM Minimum Refresh Recovery Delay Time(RFC2min).Most Significant Byte       0         797       SDRAM Minimum Refresh Recovery Delay Time(RFC2sb).Least Significant Byte       0         798       SDRAM Minimum Refresh Recovery Delay Time(RFC2sbnin).Most Significant Byte       0         799       SDRAM Minimum Refresh Recovery Delay Time(RFC2sbnin).Most Significant Byte       0         799       SDRAM Minimum Refresh Recovery Delay Time(RFC2sbnin).Most Significant Byte       0         799       RSVD,must be coded as 0x00       0         827       Advanced Memory Overclocking Features       0         828       System CMD Rate Mode       0         829       Vendor Personality Byte - RSVD       0         830       Cyclical Redundancy Code (CRC) for Base Configura tion Section, Least Significant Byte(r bytes 768–829)       0				00
797       SDRAM Minimum Refresh Recovery Delay Time(RFCsb)Least Significant Byte       0         798       SDRAM Minimum Refresh Recovery Delay Time(RFCsbmin),Most Significant Byte       0         799       SDRAM Minimum Refresh Recovery Delay Time(RFCsbmin),Most Significant Byte       0         799       SDRAM Minimum Refresh Recovery Delay Time(RFCsbmin),Most Significant Byte       0         799       Advanced Memory Overclocking Features       0         827       Advanced Memory Overclocking Features       0         828       System CMD Rate Mode       0         829       Vendor Personality Byte - RSVD       0         830       Cyclical Redundancy Code (CRC) for Base Configura tion Section, Least Significant Byte(or bytes 768-829)       0				00
798     SDRAM Minimum Refresh Recovery Delay Time(RPCsbmin),Most Significant Byte     0       799-825     RSVD,must be coded as 0x00     0       827     Advanced Memory Overclocking Features     0       828     System CMD Rate Mode     0       829     Vendor Personality Byte - RSVD     0       830     Optical Redundancy Code (CRC) for Base Configura tion Section, Least Significant Byte(for bytes 768-829)     0				00
799-826     RSVD,must be coded as 0x00     0       827     Advanced Memory Overclocking Features     0       828     System CMD Rate Mode     0       829     Vendor Personality Byte - RSVD     0       830     Cyclical Redundancy Code (CRC) for Base Configura tion Section, Least Significant Byte(for bytes 768–829)     0				
827     Advanced Memory Overclocking Features     0       828     System CMD Rate Mode     0       829     Vendor Personality Byte - RSVD     0       830     Cyclical Redundancy Code (CRC) for Base Configura tion Section, Least Significant Byte(for bytes 768–829)     0				00
828     System CMD Rate Mode     0       829     Vendor Personality Byte - RSVD     0       830     Cyclical Redundancy Code (CRC) for Base Configura tion Section, Least Significant Byte(for bytes 768–829)     0	799-826			00
829       Vendor Personality Byte - RSVD         830       Cyclical Redundancy Code (CRC) for Base Configura tion Section, Least Significant Byte(for bytes 768–829)				00
830 Cyclical Redundancy Code (CRC) for Base Configura tion Section, Least Significant Byte(for bytes 768–829)	827	Advanced Memory Overclocking Features		
				00
	828	System CMD Rate Mode		00
	828 829	System CMD Rate Mode Vendor Personality Byte - RSVD		



#### 288Pin DDR5 5600 1.1V U-DIMM 32GB Based on 2048Mx8 AQD-D5V32GN56-SB

831	Cyclical Redundancy Code (CRC) for Base Configura tion Section, Most Significant Byte(for bytes 768–829)	00
832	Profile3 Module VPP Voltage Level	00
833	Module VDD Voltage Level	00
834	Module VDDQ Voltage Level	00
835	Module TBD Voltage Level - THIS BYTE IS CURRENTLY RSVD	00
836	Memory Controller Voltage Level	00
837	SDRAM Minimum Cycle Time (tCKAVGmin)Least Significant Byte	00
838	SDRAM Minimum Cycle Time (tCKAVGmin).Most Significant Byte	00
839	SDRAM CAS Latencies Supported.First Byte	00
840	SDRAM CAS Latencies Supported, Second Byte	00
841	SDRAM CAS Latencies Supported.Third Byte	00
842	SDRAM CAS Latencies Supported Fourth Byte	00
843	SDRAM CAS Latencies Supported.Fifth Byte	00
844	RSVD for future CAS Latency	00
845	SDRAM Minimum CAS Latency Time (tAAmin),Least Significant Byte	00
846	SDRAM Minimum CAS Latency Time (tAAmin).Most Significant Byte	00
847	SDRAM Minimum RAS to CAS Delay Time (tRCDmin).Least Significant Byte	00
848	SDRAM Minimum RAS to CAS Delay Time (tRCDmin).Most Significant Byte	00
849	SDRAM Minimum Row Precharge Delay Time (RPmin)Least Significant Byte	00
850	SDRAM Minimum Row Precharge Delay Time (RPPmin).Most Significant Byte	00
851	SDRAM Minimum Active to Precharge Delay Time (RASmin).Least Significant Byte	00
852	SDRAM Minimum Active to Precharge Delay Time (IRASmin).Most Significant Byte	00
853	SDRAM Minimum Active to Active/Refresh Delay Time(RCmin) Least Significant Byte	00
854	SDRAM Minimum Active to Active/Refresh Delay Time(RCmin) Most Significant Byte	00
855	SDRAM Minimum Write Recovery Time (WRmin) Least Significant Byte	00
856	SDRAM Minimum Witte Recovery Time (WRmin).Most Significant Byte	00
857	SDRAM Minimum Refresh Recovery Delay Time(RFC1min)Least Significant Byte	00
858	SDRAM Minimum Refresh Recovery Delay Time(RFC1min).Most Significant Byte	00
859	SDRAM Minimum Refresh Recovery Delay Time(RFC2min)Least Significant Byte	00
860	SDRAM Minimum Refresh Recovery Delay Time(RFC2min).Most Significan Byte	00
861	SDRAM Minimum Refresh Recovery Delay Time(RFCsb)Least Significant Byle	00
862	SDRAM Minimum Refresh Recovery Delay Time(RFCsbmin).Most Significant Byte	00
863-890	RSVD,must be coded as 0x00	00
891	Advanced Memory Overclocking Features	00
892	System CMD Rate Mode	00
893	Vendor Personality Byte - RSVD	00
894	Cyclical Redundancy Code (CRC) for Base Configura tion Section, Least Significant Byte(for bytes 832-893)	00
895	Cyclical Redundancy Code (CRC) for Base Configura tion Section, Most Significant Bytedfor bytes 832-893)	00
896-1023	User Settings	00

Note :

1. Byte 194-201 -- By SPD Hub & PMIC Vendor & Revision

1.1 Byte 194-197 – RENESAS[ (0x80), (0xB3), (0x80), (0x21) ] ; MONTAGE[(0x86), (0x32), (0x80), (0x15)] 1.2 Byte 198-201 – RENESAS[ (0x80), (0xB3), (0x82), (0x20) ] ; RICHTEK[(0x8A), (0x8C), (0x82), (0x11)]

2. Byte 514 -- Manufacturing location by manufacturing location

3. Byte 515 -- Module manufacturing date by year (YY). (Decimal)

4. Byte 516 -- Module manufacturing date by week (WW). (Decimal )

5. Bytes 517-520 -- Module Serial Number. (Decimal)

6. Bytes 521-550 -- Module Part Number. (ASCII format, unused digits are coded as ASCII blanks (0x20).
7. Bytes 552-553 -- DRAM Manufacturer ID Code by JEDEC definition. SAMSUNG :[(0x80) ,(0xCE)]

8. Bytes 555~639 -- These bytes are undefined and can be used own purpose.