

Advantech

AQD-D5V16GN56-SB Datasheet

Rev. 1.0 2024-05-23



Description

AQD-D5V16GN56-SB is DDR5-5600(CL46)-45-45 SDRAM memory module. The SPD is programmed to JEDEC standard latency 5600Mbps timing of 46-45-45 at 1.1V. The module is composed of 16Gb CMOS DDR5 SDRAMs in FBGA package and one 8Kbit SPD Hub in 8pin TDFN package on a 288pin glass–epoxy printed circuit board.

The module is a Dual In-line Memory Module and intended for mounting onto 288 pins edge connector sockets. Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features

- RoHS compliant products.
- JEDEC standard 1.1V(1.067V~1.166V) Power supply
- VDDQ= 1.1V(1.067V~1.166V)
- VPP = 1.8V(+0.108V / -0.054V)
- Data transfer rates: PC5-5600
- Programmable CAS Latency:
 22,26,28,30,32,36,40,42,46
- 16 bit pre-fetch
- Burst Length (BL) switch on-the-fly BL16 or BC8
- Bi-directional Differential Data-Strobe
- On Die Termination, Nominal, Park
- Serial presence detect hub (SPD Hub) with Integrated Temperature sensor
- Asynchronous reset
- PCB edge connector treated with 30u" Gold-Plating

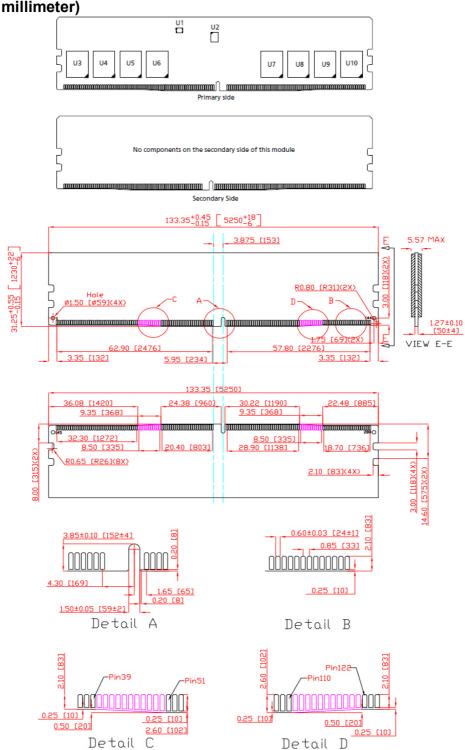


Pin Descriptions

Pin Name	Description	Pin Name	Description
CA[6:0]_A CA[6:0]_B	Address and Command Bus	DQ[31:0]_A DQ[31:0]_B	DIMM memory Data bus channel A & B
CS[1:0]_A CS[1:0]_B	Chip Select	CB[7:0]_A CB[7:0]_B	DIMM ECC Checkbits (CB) channel A & B
PAR_A PAR_B	Parity input	DQS[9:0]_A_t DQS[9:0]_B_t	Data Strobes (positive line of differential pair)
CK_t	Clocks (true/positive)	DQS[9:0]_A_c DQS[9:0]_B_c	Data Strobes (negative line of differential pair)
CK_c	Clocks (complement/negative)	TDQS[9:5]_A_t TDQS[9:5]_B_t	Not valid for x4 operation. Enabled via Mode Register.
ALERT_n	Alert for CRC error	TDQS[9:5]_A_c TDQS[9:5]_B_c	Not valid for x4 operation. Enabled via Mode Register.
RESET_n	Set DRAM to known state	VIN_BULK	DIMM Power Supply from system to PMIC
PCAMP	Control and Monitor Port	VIN_MGMT	DIMM Power Supply from system to PMIC
HSCL	I2C/I3C-Basic Host Sideband Bus Clock	VSS	Power supply return (ground)
HSDA	I2C/I3C-Basic Host Sideband Bus Data	RFU	Reserved for future use
HSA	I2C/I3C-Basic Host Sideband Bus Address	LBDQS	Loopback Data strobe output
LBDQ	Loopback Data output:		
1. TDQSx and DC	 QSx_t share a pin		



Dimensions (Unit: millimeter)



Note:1. Tolerances on all dimensions +/-0.15mm unless otherwise specified.



Pin Assignments

- 1	34	28	88-Pin DDR5	UDIN	// IM Front			288-Pin DDR5 UDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VIN_BULK	37	DQ20_A	73	CK0_A_c	109	Vss	145	VIN_BULK	181	DQ22_A	217	CK1_A_c	253	Vss
2	NC/VIN_BULK	38	Vss	74	Vss	110	DQ5_B	146	VIN_BULK	182	Vss	218	V _{SS}	254	DQ7_B
3	RFU	39	DQ21_A	75	RFU	111	V _{SS}	147	PWR_GOO D	183	DQ23_A	219	RFU	255	V _{SS}
4	HSCL	40	Vss	76	RFU	112	DQ8_B	148	HSA	184	Vss	220	RFU	256	DQ10_B
5	HSDA	41	DQ24_A	77	Vss	113	Vss	149	RFU	185	DQ26_A	221	V _{SS}	257	Vss
6	Vss	42	Vss	78	CK0_B_t	114	DQ9_B	150	Vss	186	Vss	222	CK1_B_t	258	DQ11_B
7	RFU	43	DQ25_A	79	CK0_B_c	115	Vss	151	PWR_EN	187	DQ27_A	223	CK1_B_c	259	Vss
8	Vss	44	Vss	80	Vss	116	DM1_B_n	152	RFU	188	Vss	224	Vss	260	DQS1_B_c
9	DQ0_A	45	DM3_A_n	81	RFU	117	Vss	153	Vss	189	DQS3_A_c	225	RFU	261	DQS1_B_t
10	Vss	46	Vss	82	CA12_B	118	DQ12_B	154	DQ2_A	190	DQS3_A_t	226	RFU	262	Vss
11	DQ1_A	47	DQ28_A	83	Vss	119	Vss	155	Vss	191	Vss	227	Vss	263	DQ14_B
12	Vss	48	Vss	84	CA10_B	120	DQ13_B	156	DQ3_A	192	DQ30_A	228	CA11_B	264	Vss
13	DQS0_A_c	49	DQ29_A	85	CA8_B	121	Vss	157	Vss	193	Vss	229	CA9_B	265	DQ15_B
14	DQS0_A_t	50	Vss	86	Vss	122	DQ16_B	158	DM0_A_n	194	DQ31_A	230	Vss	266	Vss
15	V _{SS}	51	CB0_A	87	CA6_B	123	Vss	159	V _{SS}	195	Vss	231	CA7_B	267	DQ18_B
16	DQ4_A	52	Vss	88	CA4_B	124	DQ17_B	160	DQ6_A	196	CB2_A	232	CA5_B	268	Vss
17	Vss	53	CB1_A	89	Vss	125	Vss	161	Vss	197	Vss	233	Vss	269	DQ19_B
18	DQ5_A	54	Vss	90	CA2_B	126	DQS2_B_c	162	DQ7_A	198	CB3_A	234	CA3_B	270	Vss
19	Vss	55	DQS4_A_c	91	CA0_B	127	DQS2_B_t	163	Vss	199	Vss	235	CA1_B	271	DM2_B_n
20	DQ8_A	56	DQS4_A_t	92	Vss	128	Vss	164	DQ10_A	200	ALERT_n	236	Vss	272	Vss
21	Vss	57	Vss	93	CS0_B_n	129	DQ20_B	165	Vss	201	Vss	237	CS1_B_n	273	DQ22_B
22	DQ9_A	58	CS0_A_n	94	Vss	130	Vss	166	DQ11_A	202	CS1_A_n	238	Vss	274	Vss
23	Vss	59	Vss	95	RESET_n	131	DQ21_B	167	Vss	203	Vss	239	DQS4_B_c	275	DQ23_B
24	DM1_A_n	60	CA0_A	96	Vss	132	Vss	168	DQS1_A_c	204	CA1_A	240	DQS4_B_t	276	Vss
25	Vss	61	CA2_A	97	CB0_B	133	DQ24_B	169	DQS1_A_t	205	CA3_A	241	Vss	277	DQ26_B
26	DQ12_A	62	Vss	98	Vss	134	Vss	170	Vss	206	Vss	242	CB2_B	278	Vss
27	Vss	63	CA4_A	99	CB1_B	135	DQ25_B	171	DQ14_A	207	CA5_A	243	Vss	279	DQ27_B
28	DQ13_A	64	CA6_A	100	Vss	136	Vss	172	Vss	208	CA7_A	244	CB3_B	280	Vss
29	Vss	65	Vss	101	DQ0_B	137	DM3_B_n	173	DQ15_A	209	Vss	245	Vss	281	DQS3_B_c
30	DQ16_A	66	CA8_A	102	Vss	138	Vss	174	Vss	210	CA9_A	246	DQ2_B	282	DQS3_B_t
31	V _{SS}	67	CA10_A	103	DQ1_B	139	DQ28_B	175	DQ18_A	211	CA11_A	247	V _{SS}	283	Vss
32	DQ17_A	68	Vss	104	Vss	140	Vss	176	Vss	212	Vss	248	DQ3_B	284	DQ30_B
33	Vss	69	CA12_A	105	DQS0_B_c	141	DQ29_B	177	DQ19_A	213	RFU	249	Vss	285	Vss
34	DQS2_A_c	70	RFU	106	DQS0_B_t	142	Vss	178	Vss	214	RFU	250	DM0_B_n	286	DQ31_B
35	DQS2_A_t	71	Vss	107	Vss	143	RFU	179	DM2_A_n	215	Vss	251	Vss	287	Vss
36	Vss	72	CK0_A_t	108	DQ4_B	144	RFU	180	Vss	216	CK1_A_t	252	DQ6_B	288	RFU

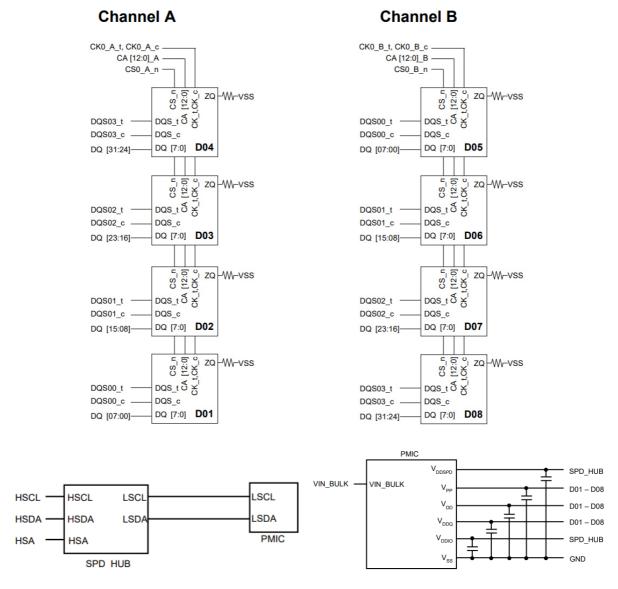
Notes:

Pin #2 is NC (No Connect) for JEDEC standard DDR5 modules. On non-standard modules used by enthusiasts that may require increased power supply, Pin #2 can be connected to VIN_BULK rail on module.



Function Block Diagram

1Rank, x8 DDR5 SDRAMs



Note : ZQ resistors are 240 Ω ± 1%.

This technical information is based on industry standard data and tests believed to be reliable. However, Advantech makes no warranties, either expressed or implied, as to its accuracy and assume no liability in connection with the use of this product. Advantech reserves the right to make changes in specifications at any time without prior notice.



Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Note
Operating Temperature	TOPER	0 to 85	°C	1,2

Note:

Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

Absolute Maximum DC Ratings

, 10001010 1110711111111 D 0 1 101111190				
Parameter	Symbol	Value	Unit	Note
Voltage on VDD relative to Vss	VDD	-0.3 ~ 1.4	V	1
Voltage on VDDQ pin relative to Vss	VDDQ	-0.3 ~ 1.4	V	1
Voltage on any pin relative to Vss	VIN, VOUT	-0.3 ~ 1.4	V	1
Storage temperature	Tstg	-55~+100	°C	1,2

Note:

- 1. Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- 2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

AC & DC Operating Conditions

Recommended DC operating conditions

Parameter	Symbol	Voltage	Rating				Notes
Parameter	Voltage		Min	Тур.	Max	Oilit	Notes
Host Supply Voltage	VIN_BULK	12.0	4.25	5.0	5.5	V	
PMIC Output Supply Voltage	VDD	1.1	1.067	1.1	1.166	V	1,2,3
PMIC Output Supply Voltage	VDDQ	1.1	1.067	1.1	1.166	V	1,2,3
PMIC Output Supply Voltage	VPP	1.8	1.746	1.8	1,908	V	3
AC Input Logic High	VIH(AC)	TBD	-	-	-	mV	
AC Input Logic Low	VIL(AC)	TBD	-	-	-	mV	
DC Input Logic High	VIH(DC)	TBD	-	-	-	mV	
DC Input Logic Low	VIL(DC)	TBD	-	-	-	mV	

Note: (1) VDD must be within 66mv of VDDQ

- (2) AC parameters are measured with VDD and VDDQ tied together.
- (3) This includes all voltage noise from DC to 2 MHz at the DRAM package ball.



IDD Specification parameters Definition - 16GB

Symbol	Condition	16GB	Unit
IDD0	One bank ACTIVATE-PRECHARGE current	TBD	mA
IDD0F	Operating Four Bank Active-Precharge Current	TBD	mA
IDD2N	Precharge Standby Current	TBD	mA
IDD2P	Precharge Power-Down Current	TBD	mA
IDD3N	Active standby current	TBD	mA
IDD3P	Active Power-Down Current	TBD	mA
IDD4R	Burst Read Current	TBD	mA
IDD4W	Burst write current	TBD	mA
IDD5B	Burst Refresh Current (1x REF)	TBD	mA
IDD5C	Burst Refresh Current (Same Bank Refresh Mode)	TBD	mA
IDD6N	Self refresh current: Normal temperature range (0–85°C)	TBD	mA
IDD7	Bank interleave read current	TBD	mA
IDD8	Maximum power-down current	TBD	mA



Timing Parameters & Specifications

		DDR5-4800 DDR5-5600			DDR5	-6400			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
			Clock	Timing					
Clock period average	tCK (AVG)	0.416	<0.454	0.357	<0.384	0.312	<0.333	ns	1
			Command and	Address Timing	9				
Read to Read command delay for same bank group	tCCD_L	max(8nCK, 5ns)	-	max(8nCK, 5ns)	-	max(8nCK, 5ns)	-	nCK,ns	8
Write to Write command delay for same bank groupp	tCCD_L_WR	max(32nCK, 20ns)	1	max(32nCK, 20ns)	-	max(32nCK, 20ns)	-	nCK,ns	8
Write to Write command delay for same bank group, second write not RMW	tCCD_L_WR2	max(16nCK,	+	max(16nCK,	-	max(16nCK,	-	nCK,ns	8
Read to Write command delay for same bank group	tCCD_L_RTW		CL - CV	VL + RBL/2 + 2tC + (tRPST - 0.5td		S offset)		nCK,ns	3,5,6,8
Write to Read command delay for same bank group	tCCD_L_WTR		C	WL + WBL/2 + M	lax(16nCK,10ns	s)		nCK,ns	4,6,8
Read to Read command delay for different bank group	tCCD_S	8	-	8	-	8	-	nCK	8
Write to Write command delay for different bank group	tCCD_S_WR	8	-	8	-	8	-	nCK	8
Read to Write command delay for different bank group	tCCD_S_RTW	CL - C\	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE						
Write to Read command delay for different bank group	tCCD_S_WTR		CWL + WBL/2 + Max(4nCK,2.5ns)						
Write to Read with Auto Precharge command delay for same bank	tCCD_WTRA			CWL + WBL/2 ·	+ tWR - tRTP			nCK,ns	2,4,6,8



		DDR5-4800		DDR5	-5600	DDR5	i-6400		
Parameter	Symbol	Min	Max	Min Max		Min	Max	Unit	Notes
Activate to Activate command delay to same bank group for 1KB page size	tRRD_L(1K)	max(8nCK, 5ns)	F	max(8nCK, 5ns)	F	max(8nCK, 5ns)	ľ	nCK,ns	8
Activate to Activate command delay to same bank group for 2KB page size	tRRD_L(2K)	max(8nCK, 5ns)	1	max(8nCK, 5ns)	1	max(8nCK, 5ns)	ı	nCK,ns	8
Activate to Activate command delay to different bank group for 1KB page size	tRRD_S(1K)	8	-	8	-	8	-	nCK	8
Activate to Activate command delay to different bank group for 2KB page size	tRRD_S(2K)	8	-	8	-	8	-	nCK	8
Four activate window for 1KB page size	tFAW (1K)	Max(32nCK,	-	Max(32nCK, 11.428ns)	-	Max(32nCK, 10.000ns)	-	nCK,ns	
Four activate window for 2KB page size	tFAW (2K)	Max(40nCK, 16.666ns)	-	Max(40nCK, 14.285ns)	-	Max(40nCK, 12.500ns)	-	nCK,ns	
Read to Precharge command delay	tRTP	Max(12nCK, 7.5ns)	-	Max(12nCK, 7.5ns)	-	Max(12nCK, 7.5ns)	-	nCK,ns	8
Precharge to Precharge command delay	tPPD	2	-	2	-	2	-	nCK	7,8
Write recovery time	tWR	30	-	30	-	30	-	ns	8



Notes:

- 1. tCK(avg)min listed for reference only, refer to the Speed Bins and Operations section which lists all valid tCK(avg) values.
- 2. tCCD_WTRA(min) shall always be greater than or equal to CWL + WBL/2 + tWR(min) tRTP(min), and when using the appropriate rounding algorithms, nCCD_WTRA(min) shall always be greater than or equal to CWL + WBL/2 + nWR(min) nRTP(min).
- 3. RBL: Read burst length associated with Read command
 - RBL = 32 (36 w/ RCRC on) for fixed BL32 and BL32 in BL32 OTF mode
 - RBL = 16 (18 w/ RCRC on) for fixed BL16 and BL16 in BL32 OTF mode
 - RBL = 16 (18 w/ RCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode
- 4. WBL: Write burst length associated with Write command
 - WBL = 32 (36 w/ WCRC on) for fixed BL32 and BL32 in BL32 OTF mode
 - WBL = 16 (18 w/ WCRC on) for fixed BL16 and BL16 in BL32 OTF mode
 - WBL = 16 (18 w/ WCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode
- 5. 5 The following is considered for tRTW equation
 - 1tCK needs to be added due to tDQS2CK
 - Read DQS offset timing can pull in the tRTW timing
 - 1tCK needs to be added when 1.5tCK postamble
- 6. CWL=CL-2
- 7. tPPD applies to any combination of precharge commands (PREab, PREsb, PREpb). tPPD also applies to any combination of precharge commands to a different die in a 3DS DDR5 SDRAM.
- 8. This parameter only specifies minimum values (there is no maximum value). The maximum value cells have been merged in the table to improve legibility.



SERIAL PRESENCE DETECT SPECIFICATION

Byte	Function Described	Fun	ction	HEX Valu
0	Number of Bytes in SPD Device	SPD Total:	1024Bytes	3
1	SPD Revision for Base Configuration Parameters		on 1.1	1
2	Key Byte / Host Bus Command Protocol Type		SDRAM	i
3	Key Byte / Host Bus Command Protocol Type Key Byte / Module Type		IMM	ď
4	First SDRAM Density and Package		16Gb	0
5	First SDRAM Addressing	Monolithic SDRAM Row: 16	Column : 10	,
6	rins districted with the world of the control of th		8	
7	First SDRAM Bank Groups & Banks Per Bank Group		nks per bank group	
8	Second SDRAM Density and Package	o bank groupsi+ ba	riks per bank group	7
9	Second SDAM Addressina			- 6
10	Secondary SDRAM I/O Width			i
11	Second SDRAM Bank Groups & Banks Per Bank Group			- 7
	decord devote beint droups a beint her beint droup			
12	SDRAM BL32 & Post Package Repair	One repair element per bank group	Burst length 32 supported	9
13	SDRAM Duty Cycle Adjuster & Partial Array Self Refresh	Device supports DCA for	4-phase internal clock(s)	(
14	SDRAM Fault Handling	Writeback suppress	sion control in MR9	(
15	Reserved	must be con	fed as 0x00	(
16	SDRAM Nominal Voltage, VDD	Operable:1.1V	Endurant:1.1V	(
17	SDRAM Nominal Voltage, VDDQ	Operable:1.1V	Endurant:1.1V	(
18	SDRAM Nominal Voltage, VPP	Operable:1.8V	Endurant:1.8V	
19	SDRAM Timing	Standard core timi		
20	SDRAM Minimum Oycle Time (tCKAVGmin), Least Significant Byte			
21	SDRAM Minimum Cycle Time (tCKAVGmin), Most Significant Byte	357	ps	
22	SDRAM Maximum Cycle Time (tCKAVGmax), Least Significant Byte			
23	SDRAM Maximum Cycle Time (tCKAVGmax), Most Significant Byte	1010	ps	
24	SDRAM CAS Latencies Supported:First Byte	CL22,26	28,30,32	
25	SDRAM CAS Latencies Supported:Second Byte		,42,46,50	-
26	SDRAM CAS Latencies Supported:Third Byte			
27	SDRAM CAS Latencies Supported Fourth Byte			
28	SDRAM CAS Latencies Supported Fifth Byte			
29	Reserved	must be con	fed as 0x00	(
30	SDRAM Minimum CAS Latency Time (AAmin), Least Significant Byte			
31	SDRAM Minimum CAS Latency Time (tAAmin), Most Significant Byte	16000	ps	
32	SDRAM Minimum RAS to CAS Delay Time (IRCDmin), Least Significant Byte	_		
33	SDRAM Minimum RAS to CAS Delay Time ((RCDmin), Most Significant Byte	16000	ps	
34	SDRAM Minimum Row Precharge Delay Time (RPmin), Least Significant Byte			
35	SDRAM Minimum Row Precharge Delay Time (RPmin), Most Significant Byte	16000	ps	
36	SDRAM Minimum Active to Precharge Delay Time (IRASmin), Least Significant Nibble			
37	SDRAM Minimum Active to Precharge Delay Time (IRASmin), Most Significant Byte	32000	ps	7
38	SDRAM Minimum Active to Active/Refresh Delay Time (RCmin), Loast Significant Nibble			
39	SDRAM Minimum Active to Active/Refresh Delay Time (RCmin), Most Significant Nibble	48000	ps	E
40	SDRAM Minimum Write Recovery Time (tWRmin), Least Significant Nibble			'
41	SDRAM Minimum Write Recovery Time (WRmin), Most Significant Nibble	30000	ps	
42	SDRAM Minimum Refresh Recovery Delay Time (RRC1min, IRRC1 strmin)Least Significant Byte			
43	SDRAM Minimum Refresh Recovery Delay Time (RPC1min, IRPC1 sir min),Most Significant Byte	295	ns	
44	SDRAM Minimum Refresh Recovery Delay Time (RPC2min, RPC2 sir min)Least Significant Byte			
45	SDRAM Minimum Refresh Recovery Delay Time (RPC2min, IRPC2 sir min) Most Significant Byte	160	ns	
46	SDRAM Minimum Refresh Recovery Delay Time (RFCsbmin, tRFCsb sir min).Least Significant Byte			
47	SDRAM Minimum Refresh Recovery Delay Time (RFCsbmin, RFCsb sir min), Most Significant Byte	130	ns	
48	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(RFC1 dir min)Least Significant Byte			
49	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank (RRC1 dir min), Most Significant Byte	monolithic SDRAMs		
50	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(tRFC2 dir min)Least Significant Byte			
51	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(RFC2 dir min), Most Significant Byte	monolithic	SDRAMs	
52	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(RPCsb dir min), Least Significant Byte			
53	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(RPCsb dir min), Most Significant Byte	monolithic	SDRAMs	
54	SDRAM Refresh Management, First Byte, First SDRAM			
55	SDRAM Refresh Management, Second Byte, First SDRAM			
56	SDRAM Refresh Management, First Byte, Second SDRAM			
57	SDRAM Refresh Management, First Byte, Second SDRAM SDRAM Refresh Management, Second Byte, Second SDRAM			
58	SDRAM Adaptive Refresh Management, First SDRAM, First ByteLevel A			
	SDRAM Adaptive Refresh Management, First SDRAM, Second Byte, Level A			
50				
59 60	SDRAM Adaptive Refresh Management, Second SDRAM, First Byte, Level A			



6.1 SCRAM Administ Reliant Assembler Assembler Standard S				
E.S. SCHOMA Advances Refusion Management, Prior SCHOMA, Prior Byte Level B				
EVALUATION CONTINUE CONTINU				00
6.4 SCRAM Advances Refund Management, Second SEDMA, Second	62	SDRAM Adaptive Refresh Management, First SDRAM, First Byte_Level B		00
6.0 SDAMA Adultive Referent Management, Stories SDAMA, Stories (Park Leve II C	63	SDRAM Adaptive Refresh Management, First SDRAM, Second Byte,Level B		00
66 SDRAM Malariter Riteria Management, Plant SDRAM, Ret Byris Space C 68 SDRAM Andrew Riteria Management, Excent SDRAM, Ret Byris, Leve C 69 SDRAM Andrew Riteria Management, Excent SDRAM, Ret Byris, Leve C 70 SDRAM Malariter Riteria Management, Excent SDRAM, Ret Byris, Leve C 71 SDRAM Malariter Affects in Article Control College Time, Same Basic Group, JRDN Lunch (Lance) Space College Colleg	64	SDRAM Adaptive Refresh Management, Second SDRAM, First Byte,Level B		00
### SCRAM Advantive Retirate Management, Resid SERMA, Second Byte, Law C ### SCRAM Advantive Retirate Management, Second SERMA, Second Byte, Law C ### SCRAM Advantive Retirate Management, Second SERMA, Second Byte, Law C ### SCRAM Advantive Retirate Management, Second SERMA, Second Byte, Law C ### SCRAM Advantive Retirate Management, Second SERMA, Second Byte, Law C ### SCRAM Advantive Active Second SERMA, Second Byte, Law C ### SCRAM Advantive Active Second SERMA, Second Byte, Law C ### SCRAM Advantive Active Second SERMA, Second Byte, Law C ### SCRAM Advantive Active Second SERMA, Second Byte, Law C ### SCRAM Advantive Active Second SERMA, Second Byte, Law C ### SCRAM Advantive Active Second SERMA SECOND LIVERAL SERVAN SECOND LIVERAL SECOND LIVE	65	SDRAM Adaptive Refresh Management, Second SDRAM, Second Byte,Level B		00
6.05 SCHAM Administration Revision Management Second SCRAM, Print Byte Leve C 7.0 SCHAM Ministration Revision Management Second SCRAM, Second Byte Leve C 7.1 SCHAM Ministration Active Active Command Data yrans, series Basic Observable Children Second Scham Ministration Active Active Command Data yrans, series Basic Observable Children Second S	66	SDRAM Adaptive Refresh Management, First SDRAM, First Byte,Level C		00
6.05 SCHAM Administration Revision Management Second SCRAM, Print Byte Leve C 7.0 SCHAM Ministration Revision Management Second SCRAM, Second Byte Leve C 7.1 SCHAM Ministration Active Active Command Data yrans, series Basic Observable Children Second Scham Ministration Active Active Command Data yrans, series Basic Observable Children Second S	67	SDRAM Adaptive Refresh Management, First SDRAM, Second Byte Level C		00
EP SERMAM Administration Management, Season Despit Services (Season Services Control), AND SERVICES (Season Services)				00
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TALL SEARCH Minimum CAS is to SEAR Command Delay Time, Same Basin Group COLD Limitions of Cold Limition of Cold Limition CAS in the Virtic CAS in Command Delay Time, Same Basin Group COLD Limitions (CAS International CAS Interna	72	SDRAM Minimum Active to Active Command Delay Time, Same Bank Group,(RRD Lmin),Lower Clock Limit	8 nCK	08
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SCRAM Minimum Park Activate Window (RFAMINIALASES) Significant Byte 11425 pc	80	SDRAM Minimum Write CAS in to Write CAS in Command Delay Time, Same Bank Group (tCCD L. WRZmin),Most. Significant Byte		27
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SURAM Minimum Park Activate Windows (RANIMINIANDES Significant Byte 30 CK	82	SDRAM Minimum Four Activate Window (IFAWmin),Least Significant Byte	44400	A4
BURNAM Minimum Final Activate Windows WRAMINIANS (WAS NOT ACTIVATED ACTIVA			11428 ps	20
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SPRAM Write to Read Command Daily to Titlement Bask Group RCDD WTRIL Lower Clock Limit			10000 ps	
BRAMA Write to Read Command Dailay for Different Bank Gloup BCCD S WTRI, Least Significant Byte 2500 ps				27
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SCHAM Write to Read Command Delay to Entered Bank Group (CCD is WTRI, Most Significant Byte 4 CCK	88	SDRAM Write to Read Command Delay for Different Bank Group (tCCD S WTR), Least Significant Byte	2500 00	C4
SDRAM Read to Procharge Command Daisy STEP, STEP str), Least Significant Byte 7500 ps	89	SDRAM Write to Read Command Delay for Different Bank Group (tCCD 'S WTR), Most Significant Byte	2000 ps	09
SDRAM Read to Precharge Command Delay SRTP, SRTP stry Last Significant Byte 7500 ps	90	SDRAM Write to Read Command Delay for Different Bank Group,(tCCD S. WTR), Lower Clock Limit	4 nCK	04
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198 PMIC O Manufacturer ID Code, Second Byte 200 PMIC O Device Type 201 PMIC O Revision Number 202 PMIC 1 Manufacturer ID Code, First Byte 203 PMIC 1 Manufacturer ID Code, Second Byte 204 PMIC 1 Device Type 205 PMIC 1 Device Type 206 PMIC 2 Manufacturer ID Code, Second Byte 207 PMIC 2 Manufacturer ID Code, Second Byte 208 PMIC 2 Manufacturer ID Code, Second Byte 209 PMIC 2 Manufacturer ID Code, Second Byte 200 PMIC 2 Manufacturer ID Code, Second Byte 201 Themal Sensor Manufacturer ID Code, Second Byte 202 Themal Sensor Manufacturer ID Code, Second Byte 210 Themal Sensor Manufacturer ID Code, Second Byte 211 Themal Sensor Revision Number 212 Themal Sensor Revision Number 213 Themal Sensor Revision Number 214 DRAM Specification Level 215 SPD Specification Level 216 PMICC1 Specification Level 217 PMICC1 Specification Level	197	SPD Device Revision Number	By SPD, Hub & PMIC Vendor & Revision	
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PMIC 0 Revision Number 201 PMIC 1 Manufacturer ID Code, First Byte 203 PMIC 1 Manufacturer ID Code, Second Byte 204 PMIC 1 Device Type 205 PMIC 1 Revision Number 206 PMIC 2 Manufacturer ID Code, Second Byte 207 PMIC 2 Manufacturer ID Code, Second Byte 208 PMIC 2 Device Type 209 PMIC 2 Povice Type 209 PMIC 2 Device Type 200 PMIC 2 Device Type 201 Thermal Sensor Manufacturer ID Code, First Byte 211 Thermal Sensor Manufacturer ID Code, Second Byte 212 Thermal Sensor Manufacturer ID Code, Second Byte 213 Thermal Sensor Povice Type 214 DRAM Specification Level 215 SPD Specification Level 216 PMIC 9 Specification Level 217 PMIC1 Specification Level	400	DMC 0 Magnifeshier ID Code Second Buts		\vdash
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PMIC 1 Manufacturer ID Code, First Byte 203 PMIC 1 Manufacturer ID Code, Second Byte 204 PMIC 1 Device Type 205 PMIC 2 Manufacturer ID Code, First Byte 206 PMIC 2 Manufacturer ID Code, First Byte 207 PMIC 2 Manufacturer ID Code, Second Byte 208 PMIC 2 Device Type 209 PMIC 2 Revision Number 210 Thermal Sensor Manufacturer ID Code, First Byte 211 Thermal Sensor Manufacturer ID Code, Second Byte 212 Thermal Sensor Manufacturer ID Code, Second Byte 213 Thermal Sensor Revision Number 214 DRAM Sensor Revision Number 215 SPD Specification Level 216 PMICO Specification Level 217 PMIC1 Specification Level	200	PMIC 0 Device Type		1 .
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203 PMIC 1 Manufacturer ID Code, Second Byte 204 PMIC 1 Device Type 205 PMIC 1 Revision Number 206 PMIC 2 Manufacturer ID Code, First Byte 207 PMIC 2 Manufacturer ID Code, Second Byte 208 PMIC 2 Device Type 209 PMIC 2 Device Type 209 PMIC 2 Revision Number 210 Thermal Sensor Manufacturer ID Code, First Byte 211 Thermal Sensor Manufacturer ID Code, Second Byte 212 Thermal Sensor Manufacturer ID Code, Second Byte 213 Thermal Sensor Navision Number 214 Thermal Sensor Revision Number 215 SPD Specification Level 216 PMICO Specification Level 217 PMICO Specification Level 218 PMICO Specification Level 219 PMICO Specification Level	$\overline{}$			00
204 PMIC 1 Device Type 205 PMIC 1 Revision Number 206 PMIC 2 Manufacturer ID Code, First Byte 207 PMIC 2 Manufacturer ID Code, Second Byte 208 PMIC 2 Device Type 209 PMIC 2 Revision Number 210 Thermal Sensor Manufacturer ID Code, First Byte 211 Thermal Sensor Manufacturer ID Code, Second Byte 212 Thermal Sensor Manufacturer ID Code, Second Byte 213 Thermal Sensor Revision Number 214 ORAM Specification Level 215 SPD Specification Level 216 PMICO Specification Level 217 PMICI Specification Level	-			
205 PMIC 2 Manufacturer ID Code, First Byte 207 PMIC 2 Manufacturer ID Code, Second Byte 208 PMIC 2 Device Type 209 PMIC 2 Revision Number 210 Thermal Sensor Manufacturer ID Code, Second Byte 211 Thermal Sensor Manufacturer ID Code, Second Byte 212 Thermal Sensor Device Type 213 Thermal Sensor Revision Number 214 Sensor Revision Number 215 Sensor Revision Number 216 PMIC 2 Specification Level 217 PMIC 1 Specification Level 218 PMIC 2 Specification Level 219 PMIC 1 Specification Level				00
206 PMIC 2 Manufacturer ID Code, First Byte 207 PMIC 2 Manufacturer ID Code, Second Byte 208 PMIC 2 Device Type 209 PMIC 2 Revision Number 210 Thermal Sensor Manufacturer ID Code, Second Byte 211 Thermal Sensor Manufacturer ID Code, Second Byte 212 Thermal Sensor Device Type 213 Thermal Sensor Revision Number 214 DRAM Specification Level 215 SPD Specification Level 216 PMICO Specification Level 217 PMICI Specification Level				00
207 PMIC 2 Manufacturer ID Code, Second Byte 208 PMIC 2 Device Type 209 PMIC 2 Revision Number 210 Thermal Sensor Manufacturer ID Code, First Byte 211 Thermal Sensor Manufacturer ID Code, Second Byte 212 Thermal Sensor Device Type 213 Thermal Sensor Revision Number 214 DRAM Specification Level 215 SPD Specification Level 216 PMICO Specification Level 217 PMIC1 Specification Level	205	PMIC 1 Revision Number		00
208 PMIC 2 Device Type	206	PMIC 2 Manufacturer ID Code, First Byte		00
208 PMIC 2 Device Type	207	PMIC 2 Manufacturer ID Code, Second Byte		00
209 PMiC 2 Revision Number 210 Thermal Sensor Manufacturer ID Code, First Byte 211 Thermal Sensor Manufacturer ID Code, Second Byte 212 Thermal Sensor Device Type 213 Thermal Sensor Revision Number 214 DRAM Specification Level 215 SPD Specification Level 216 PMiCO Specification Level 217 PMiC1 Specification Level				00
210 Thermal Sensor Manufacturer ID Code, First Byte 211 Thermal Sensor Manufacturer ID Code, Second Byte 212 Thermal Sensor Device Type 213 Thermal Sensor Revision Number 214 DRAM Specification Level 215 SPD Specification Level 216 PMICO Specification Level 217 PMICI Specification Level				00
211 Thermal Sensor Manufacturer ID Code, Second Byte 212 Thermal Sensor Device Type 213 Thormal Sensor Revision Number 214 DRAM Specification Level 215 SPD Specification Level 216 PMICO Specification Level 217 PMICI Specification Level	-			00
212 Thermal Sensor Device Type 213 Thermal Sensor Revision Number 214 DRAM Specification Level 215 SPD Specification Level 216 PMICO Specification Level 217 PMIC1 Specification Level				
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214 DRAM Specification Level 215 SPD Specification Level 216 PMICO Specification Level 217 PMICI Specification Level				00
215 SPD Specification Level 216 PMICO Specification Level 217 PMICO Specification Level	213	Thermal Sensor Revision Number		00
215 PMICO Specification Level 217 PMICO Specification Level	214	DRAM Specification Level		00
215 PMICO Specification Level 217 PMICO Specification Level				00
217 PMIC1 Specification Level				00
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210 IF MICC ODMINICATION LAYER				00
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219 TS Specification Level		•		00
220 DIMM Specification Level	220	DIMM Specification Level		r 00



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1.150mm	221-229	Reserved	Reserved	00
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Description Processing Pr				01
Section Sect				00
Description				81
Section Sect				
Section Sect	234	(Unbuffered): Module Organization		00
	235	Memory Channel Bus Width	2 channels/32 bits	22
Associated for Author uses	236-239	Reserved	must be coded as 0x00	00
Color De la gran - Color De la	240-447	(Unbuffered):Module Type Specific Information	Reserved	00
CRC Marie System CRC System System CRC	448-509	Reserved for future use		00
Maria Manufacturer D Cook, Prot Byte Advantacturer D Cook, Prot Byte	510	CRC for Byte 0-509, Least Significant Byte	CRC	-
Mail	511	CRC for Byte 0-509,Most Significant Byte	CRC	-
Marie Manufacturer Colons, Second Byte 1960 1960 2	512	Module Manufacturer ID Code, First Byte		8A
154			Advantech	C8
Stock Manufacturing Date "Neat 4 (Declinary)			*Note: 2	
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1918				٠.
Module Serial Number Module Serial Number		THE CONTRACTOR STREET	Product 4 (processing)	
190				\vdash
1920 1921 1922		Module Serial Number	*Note: 5 (Decimal)	
1921 1922 1923 1924 1925				<u> </u>
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1972 1973 1974				<u> </u>
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1999 1999				<u> </u>
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S33	530			
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Module Part Number	534			
538 539 538 539 540 541 541 542 543 543 544 545 546	535	Market Start Number	Make 5	-
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545 546 547 548 549 550 551 Module Revision Code 552 DRAM Manufacturer ID Code, First Byte 553 DRAM Manufacturer ID Code, Second Byte 554 DRAM Stepping 555 DRAM Stepping 556 DRAM Stepping 556 DRAM Stepping 556 DRAM Stepping 561 DRAM Stepping 562 DRAM Stepping 563 DRAM Stepping 564 DRAM Stepping 565 DRAM Stepping 566 DRAM Stepping 566 DRAM Stepping 566 DRAM Stepping 567 DRAM Stepping 568 DRAM Stepping 568 DRAM Stepping 569 DRAM Stepping 560 DRAM S				<u> </u>
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548				<u> </u>
549				<u> </u>
550 Module Revision Code 551 Module Revision Code 552 DRAM Manufacturer ID Code, First Byte 553 DRAM Manufacturer ID Code, Second Byte 554 DRAM Stepping 555-639 Manufacturer's Specific Data 565-639 Manufacturer's Specific Data 565-639 Manufacturer's Specific Data 565-639 Manufacturer's Specific Data 565-639 Manufacturer's Specific Data 566-639 Manufacturer's S				<u> </u>
551 Module Revision Code 552 DRAM Manufacturer ID Code, First Byte Samsung 8 553 DRAM Manufacturer ID Code, Second Byte Samsung C 554 DRAM Stepping Samsung C 555-639 Manufacturer's Specific Data *Note: 7 640 Intel Extreme Memory Profile Identification String C 641 Intel Extreme Memory Profile Identification String C 642 Intel Extreme Memory Profile Version C 643 Intel Extreme Memory Profile Configuration C 644 Intel Extreme Memory Profile Configuration C 645 PMIC Vendor ID C 645 PMIC Vendor ID C 646 PMIC Vendor ID C 647 PMIC Vendor ID C 648 PMIC Vendor ID C 649 PMIC Vendor ID C 640 C 641 PMIC Vendor ID C 642 PMIC Vendor ID C 644 PMIC Vendor ID C 645 PMIC Vendor ID C 646 PMIC Vendor ID C 647 PMIC Vendor ID C 648 PMIC Vendor ID C 649 PMIC Vendor ID C 640 PMIC Vendor ID C 640 PMIC Vendor ID C 641 PMIC Vendor ID C 644 PMIC Vendor ID C 645 PMIC Vendor ID C 646 PMIC Vendor ID C 647 PMIC Vendor ID C 648 PMIC Vendor ID C 649 PMIC Vendor ID C 640 PMIC Vendor ID C 641 PMIC Vendor ID C 642 PMIC Vendor ID C 643 PMIC Vendor ID C 644 PMIC Vendor ID C 645 PMIC Vendor ID C 646 PMIC Vendor ID C 647 PMIC Vendor ID C 648 PMIC Vendor ID C 649 PMIC Vendor ID C 640 PMIC Vendor ID C 641 PMIC Vendor ID C 642 PMIC Vendor ID C 643 PMIC Vendor ID C 644 PMIC Vendor ID C 645 PMIC Vendor ID C 646 PMIC Vendor ID C 647 PMIC Vendor ID C 648 PMIC Vendor ID C 649 PMIC Vendor ID C 640 PMIC Vendor ID C 641 PMIC Vendor ID C 641 PMIC Vendor ID C 642 PMIC Vendor ID C 643 PMIC Vendor ID C 644 PMIC Vendor ID C 645 PMIC Vendor ID C 646 PMIC Vendor ID C 647 PMIC Vendor ID C 648 PMIC Vendor ID C 649 PMIC Vendor ID C 640 PMIC Vendor ID C 641 PMIC Vendor ID C				\vdash
552 DRAM Manufacturer ID Code, First Byte Samsung C		Made Parisher Code		
553 DRAM Manufacturer ID Code, Second Byte Samsung C				00
553 DRAM Manufacturer ID Code, Second Byte St.			Samsung	80
555-639 Manufacturer's Specific Data				CE
640 Intel Extreme Memory Profile Identification String				95
641 Intel Extreme Memory Profile Identification String 642 Intel Extreme Memory Profile Version 643 Intel Extreme Memory Profile Cognization 644 Intel Extreme Memory Profile Configuration 645 PMIC Vendor ID 665 PMIC Vendor ID			*Note: 7	
642 Intel Extreme Memory Profile Version 0 643 Intel Extreme Memory Profile Organization 0 644 Intel Extreme Memory Profile Configuration 0 645 PMIC Vendor ID 0		·		00
643 Intel Extreme Memory Profile Organization 0 644 Intel Extreme Memory Profile Configuration 0 645 PMIC Vendor ID 0		Intel Extreme Memory Profile Identification String		00
644 Intel Extreme Memory Profile Configuration 645 PMIC Vendor ID 667	642	Intel Extreme Memory Profile Version		00
645 PMIC Vendor ID 0	643	Intel Extreme Memory Profile Organization		00
	644	Intel Extreme Memory Profile Configuration		00
	645	PMIC Vendor ID		00
	646	PMIC Vendor ID		00



Enabling an Intelligent Planet

647	Number of PMICs	 00
648	PMIC Capabilities	 00
849-853	RSVD	00
654		00
655	1	00
656	'	00
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660		00
661	第3頁	00
662	Profile 1 String Name	00
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694	Profile 3 String Name	00
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698	.	00
699	.	00
700	.	00
701	.	00
	Cyclical Redundancy Code (CRC) for Base Configuration Section, Least Significant Byte (for bytes 640–701)	00
	Cyclical Redundancy Code (CRC) for Base Configuration Section, basis arginificant Byte (for bytes 640–701) Cyclical Redundancy Code (CRC) for Base Configuration Section, Most Significant Byte (for bytes 640–701)	00
		00
	Profile 1 : Module VPP Voltage Level Module VDD Voltage Level	00
	Module VDDQ Veltage Level	00
	Module TBD Voltage Level - THIS BYTE IS CURRENTLY RSVD	00
	Memory Controller Voltage Level	00
	SDRAM Minimum Cycle Time (tCKAVGmin),Least Significant Byte	00
	SDRAM Minimum Cycle Time (tCKAVGmin),Most Significant Byte	00
	SDRAM CAS Latencies Supported,First Byte	00
	SDRAM CAS Latencies Supported,Second Byte	00
713	SDRAM CAS Latencies Supported, Third Byte	00
714	SDRAM CAS Latencies Supported,Fourth Byte	00



714	SDRAM CAS Latencies Supported.Fourth Byte		00
715	SDRAM CAS Latencies Supported Fifth Byte		00
716	RSVD for future CAS Latency		00
717	SDRAM Minimum CAS Latency Time (tAamin)Least Significant Byte		00
718	SDRAM Minimum CAS Latency Time (t-Amin) Most Significant Byte	1	00
719	SDRAM Minimum RAS to CAS Delay Time (IRCOmin)Least Significant Byte		00
720	SDRAM Minimum RAS to CAS Delay Time (RCDmin),Most Significant Byte		00
721	SDRAM Minimum Row Precharge Delay Time (tRCDmin),Least Significant Byte		00
-			00
722	SDRAM Minimum Row Precharge Delay Time (RPmin),Most Significant Byte		
723	SDRAM Minimum Active to Precharge Delay Time (tRASmin).Least Significant Byte		00
724	SDRAM Minimum Active to Precharge Delay Time (RASmin) Most Significant Byte		00
725	SDRAM Minimum Active to Active/Refresh Delay Time(tRCmin) Least Significant Byte		00
726	SDRAM Minimum Active to Active/Refresh Delay Time(tRCmin) ,Most Significant Byte		00
727	SDRAM Minimum Write Recovery Time (tWRmin),Least Significant Byte		00
728	SDRAM Minimum Write Recovery Time (tWRmin),Most Significant Byte		00
729	SDRAM Minimum Refresh Recovery Delay Time(RFC1min),Least Significant Byte		00
730	SDRAM Minimum Refresh Recovery Delay Time(tRFC1min),Most Significant Byte		00
731	SDRAM Minimum Refresh Recovery Delay Time(RFC2min),Least Significant Byte		00
732	SDRAM Minimum Refresh Recovery Delay Time(RFC2min) Most Significant Byte		00
733	SDRAM Minimum Refresh Recovery Delay Time(RFCsb),Least Significant Byte		00
734	SDRAM Minimum Refresh Recovery Delay Time(RFCsbmin),Most Significant Byte		00
735-762	RSVD,must be coded as 0x00		00
763	Advanced Memory Overclocking Features		00
764	System CMD Rate Mode		00
765	Vendor Personality Byte - RSVD		00
766	Cyclical Redundancy Code (CRC) for Base Configuration Section, Least Significant Busingfor bytes 704–765)		00
767	Cyclical Redundancy Code (CRC) for Base Configura tion Section, Most Symhifteent, By terior bytes 704–765)		00
768	Profile2: Module VPP Voltage Level		00
769	Module VDD Voltage Level		00
770	Module VDDQ Voltage Level		00
771			00
772	Module TBD Voltage Level - THIS BYTE IS CURRENTLY RSVD Memory Controller Voltage Level		00
773			00
	SDRAM Minimum Cycle Time (tCKAVGmin).Least Significant Byte		00
774	SDRAM Minimum Cycle Time (tCKAVGmin),Most Significant Byte		
775	SDRAM CAS Latencies Supported First Byte		00
776	SDRAM CAS Latencies Supported, Second Byte		00
777	SDRAM CAS Latencies Supported, Third Byte	*	00
778	SDRAM CAS Latencies Supported,Fourth Byte	•	00
779	SDRAM CAS Latencies Supported,Fifth Byte	•	00
780	RSVD for future CAS Latency		00
781	SDRAM Minimum CAS Latency Time (tAAmin),Least Significant Byte		00
782	SDRAM Minimum CAS Latency Time (tAAmin),Most Significant Byte		00
783	SDRAM Minimum RAS to CAS Delay Time (IRCDmin) Least Significant Byte		00
784	SDRAM Minimum RAS to CAS Delay Time (RCDmin),Most Significant Byte		00
785	SDRAM Minimum Row Precharge Delay Time (RPmin),Least Significant Byte		00
786	SDRAM Minimum Row Precharge Delay Time (RPmin) Most Significant Byte]	00
787	SDRAM Minimum Active to Precharge Delay Time (RASmin)Least Significant Byte		00
788	SDRAM Minimum Active to Precharge Delay Time (tRASmin) Most Significant Byte	1	00
789	SDRAM Minimum Active to Active/Refresh Delay Time(RCmin) ,Least Significant Byte		00
790	SDRAM Minimum Active to Active/Refresh Delay Time(IRCmin), Most Significant Byte	1	00
791	SDRAM Minimum Write Recovery Time (WRmin)Least Significant Byte		00
792	SDRAM Minimum Write Recovery Time (tWRmin) Most Significant Byte	1	00
793	SDRAM Minimum Refresh Recovery Delay Time(RFC1min)Loast Significant Byte		00
794	SDRAM Minimum Refresh Recovery Delay Time(RPC1min) Most Significant Byte	1	00
795	SDRAM Minimum Refresh Recovery Delay Time(RFC2min)Least Significant Byte		00
796	SDRAM Minimum Refresh Recovery Delay Time(RFC2min),Most Significant Byte	1	00
			00
797	SDRAM Minimum Refresh Recovery Delay Time(RFCsb),Least Significant Byte		
798	SDRAM Minimum Refresh Recovery Delay Time(RPCsbmin).Most Significant Byte		00
799-826			00
827	Advanced Memory Overclocking Features		00
828	System CMD Rate Mode		00
	Vendor Personality Byte - RSVD	I	00
829			_
830 831	Vertical Redundancy Code (CRC) for Base Configura tion Section, Least Significant Byte(for bytes 768–829) Cyclical Redundancy Code (CRC) for Base Configura tion Section, Most Significant Byte(for bytes 768–829)		00



288Pin DDR5 5600 1.1V U-DIMM 16GB Based on 2048Mx8 AQD-D5V16GN56-SB

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832	Profile3 :Module VPP Voltage Level		00
833	Module VDD Voltage Level		00
	Module VDDQ Voltage Level		00
835	Module TBD Voltage Level - THIS BYTE IS CURRENTLY RSVD		00
836	Memory Controller Voltage Level		00
837	SDRAM Minimum Cycle Time (tCKAVGmin),Least Significant Byte		00
838	SDRAM Minimum Cycle Time (tCKAVGmin),Most Significant Byte		00
839	SDRAM CAS Latencies Supported, First Byte		00
840	SDRAM CAS Latencies Supported, Second Byte		00
841	SDRAM CAS Latencies Supported, Third Byte		00
842	SDRAM CAS Latencies Supported, Fourth Byte		00
843	SDRAM CAS Latencies Supported, Fifth Byte		00
844	RSVD for future CAS Latency		00
845	SDRAM Minimum CAS Latency Time (tAAmin),Least Significant Byte		00
846	SDRAM Minimum CAS Latency Time (tAAmin),Most Significant Byte		00
847	SDRAM Minimum RAS to CAS Delay Time (RCDmin),Least Significant Byte		00
848	SDRAM Minimum RAS to CAS Delay Time (RCDmin) Most Significant Byte		00
849	SDRAM Minimum Row Precharge Delay Time (RPmin),Least Significant Byte		00
850	SDRAM Minimum Row Precharge Delay Time (RPmin),Most Significant Byte		00
851	SDRAM Minimum Active to Precharge Delay Time (tRASmin),Least Significant Byte		00
852	SDRAM Minimum Active to Precharge Delay Time (IRASmin),Most Significant Byte		00
853	SDRAM Minimum Active to Active/Refresh Delay Time(tRCmin) ,Least Significant Byte		00
854	SDRAM Minimum Active to Active/Refresh Delay Time(RCmin) ,Most Significant Byte		00
855	SDRAM Minimum Write Recovery Time (tWRmin)Least Significant Byte		00
856	SDRAM Minimum Write Recovery Time (WRmin) Most Significant Byte		00
857	SDRAM Minimum Refresh Recovery Delay Time(RFC1min)Least Significant@yte		00
858	SDRAM Minimum Refresh Recovery Delay Timet/RFC1min) Most Significant Byte		00
	SDRAM Minimum Refresh Recovery Delay Time(tRFC/2min)Least Significant Byte		00
	SDRAM Minimum Refresh Recovery Delay Time(tRFC/zmin).Most Significant Byte		00
861	SDRAM Minimum Refresh Recovery Delay Time(RFCsb)Least Significant Byte		00
862	SDRAM Minimum Refresh Recovery Delay Time(tRFCsbmin) Most Significant Byte		00
863-890	RSVD.must be coded as 0x00	'	00
	Advanced Memory Overclocking Features		00
	System CMD Rate Mode		00
	Vendor Personality Byte - RSVD		00
	Cyclical Redundancy Code (CRC) for Base Configura tion Section, Least Significant Byte(for bytes 832–893)		00
	Oyclical Redundancy Code (CRC) for Base Configuration Section, Most Significant Byteffor bytes 832-893)		00
	User Settings		00
Noto:			-

Note:

- 1. Byte 194-201 -- By SPD Hub & PMIC Vendor & Revision
- 1.1 Byte 194-197 RENESAS[(0x80), (0xB3), (0x80), (0x21)]; MONTAGE[(0x86), (0x32), (0x80), (0x15)] 1.2 Byte 198-201 RENESAS[(0x80), (0xB3), (0x82), (0x20)]; RICHTEK[(0x8A), (0x8C), (0x8C), (0x11)]
- 2. Byte 514 -- Manufacturing location by manufacturing location
- 3. Byte 515 -- Module manufacturing date by year (YY). (Decimal)
- 4. Byte 516 -- Module manufacturing date by week (WW). (Decimal)
- 5. Bytes 517-520 -- Module Serial Number. (Decimal)
- 6. Bytes 521-550 -- Module Part Number. (ASCII format, unused digits are coded as ASCII blanks (0x20).
 7. Bytes 552-553 -- DRAM Manufacturer ID Code by JEDEC definition. SAMSUNG :[(0x80) ,(0xCE)]
- 8. Bytes 555~639 -- These bytes are undefined and can be used own purpose