## 產品承認書

## (APPROVAL SHEET)

公司名稱 (Customer):研華股份有限公司

產品名稱 (Part Description): SSD 固態硬碟

製造原廠 (Manufacture): <u>光寶科技股份有限公司</u>

光寶品名 (Model Name): CV8-8E128-72、CV8-8E256-72、CV8-8E512-72

光寶料號及FW對照表:

Model Name	LiteON PN / Advantech PN	Firmware Version
CV8-8E128-72	3C07110223 / 96FD80-NT128-LIS	1.00
CV8-8E256-72	3C07120343 / 96FD80-NT256-LIS	1.00
CV8-8E512-72	3C07140182 /96FD80-NT512-LIS	1.00

晶片廠牌 (Chip brand): SMI 2258 + Toshiba Flash BiCS3 3D TLC

Density:	128/256/512 GB	Interface:	SATA 6.0 Gb/s			
From Factor:	M.2 2280	Voltage / Current:	3.3 V / 0.95A			
Ambient Non-OP Temp:	-40~+85°C	Ambient OP Temp:	0~70°C			
	CUSTOMER APPROVAL BY					

### LITE-ON TECHNOLOGY CORPORATION



# LTEON

## CV8-8EXXX

Model

CV8-8E128

CV8-8E256

CV8-8E512

## M.2 2280

## SATA 6.0 Gb/s Solid State Drive

## **Product Specification**

Manual Rev.:

Rev 1.0

Revision Date: 2017/10/25

**Prodcut Specification** 



#### **Document History**

Revision	Date	Changes
Rev 1.0	2017/10/25	First release



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## LTEON

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## LTEON

## **1** Introduction

#### 1.1 Overview :

The **CV8-8EXXX 3D TLC** series mSATA second generation (M.2) SATA 6Gb/s Solid State Drive (SSD) delivers leading performance in an industry standard M.2 type 2280-S3-B-M form factor while simultaneously improving system responsiveness for mobile applications over standard rotating drive media or hard disk drives. By combining leading NAND flash memory technology with our innovative high performance firmware, LITEON delivers a SSD for native Serial Advanced Technology Attachment (SATA) hard disk drive drop-in replacement with enhanced performance, reliability, ruggedness and power savings. Since there are no rotating platters, moving heads, fragile actuators, or unnecessary delays due to spin-up time or positional seek time that can slow down the storage subsystem, significant I/O and throughput performance improvement is achieved as compared to rotating media or hard disk drives. This document describes the specifications of the **CV8-8EXXX 3D TLC** series M.2 SSD in M.2 type 2280-S3-B-M form factors.

The **CV8-8EXXX 3D TLC** M.2 SSD primarily targets M.2 based laptop PCs, highly rugged mobile client devices, as well as thin and light mini/sub-notebooks. Key attributes include high performance, low power, increased system responsiveness, high reliability, and enhanced ruggedness as compared to standard mobile M.2 hard drives. The **CV8-8EXXX 3D TLC** M.2 SSD is available in M.2 type 2280-S3-B-M form factor that are electrically, mechanically, and software compatible with existing M.2 slots. Our flexible design allows interchangeability with existing mobile hard drives based on the M.2 interface standard.

#### 1.2 Product Specification

#### 1.2.1. Form Factor:

128/256/512GB: M.2 type 2280-S3-B-M SSD form factor

#### 1.2.2. Capacity:

N	lodel	Unformatted capacity	Total user addressable sectors in LBA mode
CV8	8-8E128	128GB	250,069,680
CV8	3-8E256	256GB	500,118,192
CV8	3-8E512	512GB	1,000,215,216

#### Table 1 User Addressable Sectors

Notes:

- 1. 1GB=1,000,000,000 bytes and not all of the memory can be used for storage.
- 2. 1 Sector = 512 bytes

1.2.3. Flash: 3D Triple-Level Cell (TLC) component with Toggle-Mode



#### 1.2.4. Band Performance

Table 2 Maximum Sustained Read and Write Bandwidth

Capacity	Access Type	MB/s
128 GB	Sequential Read	Up to 550
	Sequential Write	Up to 380
256 GB	Sequential Read	Up to 550
	Sequential Write	Up to 450
512 GB	Sequential Read	Up to 550
	Sequential Write	Up to 450

#### Notes:

- 1. Performance measured using CrystalDiskMark 5.0.3
- 1 MB/sec = 1,048,576 bytes/sec is used in measuring sequential performance.
   If 1 MB/sec = 1,000,000 bytes/sec is used, performance values become 4.85% higher.
- 3. Test platform: ASUS P8P67 PRO (Windows 7 x64)
- 4. Test by secondary drive (data drive) under SATA 6Gb/s.
- 5. Actual performance may vary depending on use conditions and environment.

#### 1.2.5. Read and Write IOPS (IOMETER)

#### Table 3 Random Read/Write Input/Output Operations per Second

Capacity	Access Type	IOPS
128GB	4K Random Read	70,000
	4K Random Write	40,000
256GB	4K Random Read	90,000
	4K Random Write	68,000
512GB	4K Random Read	90,000
	4K Random Write	70,000

#### Notes:

- 1. Performance measured using IOMETER with queue depth set to 32,
- 2. Write cache enabled.
- 3. Test platform: ASUS P8P67 PRO (Windows 7 x64)
- 4. Test by secondary drive (data drive) under SATA 6Gb/s.
- 5. Actual performance may vary depending on use conditions and environment.

#### 1.2.6. Ready Time

#### **Table 4 Latency Specifications**

Туре	Average Latency
Power on to Ready	500ms
Resume from DEVSLP	100ms

#### Notes:

- 1. Device measured form power-on to ready to receive first Media command
- 2. Power On To Ready time assumes drive have normal shutdown process which have STANDBY IMMEDIATE command. Time varies if shutdown is not preceded by



#### 1.2.7. Power Management

-- SATA interface power management

#### 1.2.8. Power Consumption

#### **Table 5 Operating Voltage**

Capacity	Description	Min	Max	Unit
128GB	Operating voltage for 3.3V (+/- 5%)	3.135	3.465	V
256GB	Operating voltage for 3.3V (+/- 5%)	3.135	3.465	V
512GB	Operating voltage for 3.3V (+/- 5%)	3.135	3.465	V

#### Table 6 Power Consumption (MobileMark)

256GB	Operating voltage for 3.3V (+/- 5%)		3.135	3.465	V	
512GB	Operating voltage for 3.3V (+/- 5%)		3.135	3.465	V	
Table 6 Power Consumption (MobileMark)						
Capacity	Mode	Max		Unit	t	
128GB	DIPM Enable	0.25		W		
256GB	DIPM Enable	0.25		W		
512GB	DIPM Enable	0.25		W		

#### Table 7 DEVSLP Mode Power Consumption

Capacity	Mode	Max	Unit
128GB	DEVSLP	3	mW
256GB	DEVSLP	3	mW
512GB	DEVSLP	3	mW

#### 1.2.9. Temperature

#### **Table 8 Temperature Relative Specifications**

Environment	Mode	Min	Мах	Unit
Ambient	Operating	0	70	°C
Temperature	Non-operating	-40	85	°C
Humidity	Operation	5	95	%
Humidity	Non-operation	5	95	%

Note: Measured without condensation

#### 1.2.10. Compatibility

-- SATA Revision 3.0 compliant

Compatible with SATA 1.5Gb/s, 3.0Gb/s & 6.0Gb/s interface rates

- -- ATA/ATAPI- 8 compliant
- -- SSD enhanced SMART ATA feature set
- -- Native Command Queuing (NCQ) command set
- -- TRIM supported



#### 1.2.11. Certifications

#### **Table 9 Device Certifications**

Certification	Description
	Indicates conformity with the essential health and safety
CE compliant	requirements set out in European Directives Low voltage
	Directive and EMC Directive
UL certified	Underwriters Laboratories, Inc. Component Recognition
OLCEITINEU	UL60950-1
	Compliance to the Taiwan EMC standard "Limits and methods of
BSMI	Radio Disturbance Characteristics of Information Technology
	Equipment, CNS 13438 Class B"
Microsoft WHQL	Microsoft Windows Hardware Quality Labs
<b>RoHS</b> compliant	Restriction of Hazardous Substance Directive

#### 1.2.12. Reliability

#### **Table 10 Reliability specifications**

Parameter	Value
Mean Time between Failure (MTBF)	> 1,500,000 hours
Power on/off cycles	50000 cycles

#### Notes:

- 1. MTBF is calculated based on a Part Stress Analysis. It assumes nominal voltage. With all other parameters within specified range.
- 2. Power on/off cycles is defined as power being removed from the drive, and the restored. Most host systems remove power from the drive when entering suspend and hibernate as well as on a system shutdown.

#### 1.2.13. Shock and Vibration

ltem	Mode	Timing/Frequency	Max
Shock	operating	At 1 msec half-sine	1500G
	operating	At 2 msec half-sine	1000G
	Non-operating	At 1 msec half-sine	1500G
	Non-operating	At 2 msec half-sine	1000G
Vibration	Operation	7~800 Hz	3.08Grms
	Non-operation	20~2000 Hz	16.3Grms

Table 11 Shock and Vibration

#### Notes:

- 1. Shock specifications assume that the SSD is mounted securely with the input vibration applied to the drive mounting screws. Stimulus may be applied in the X, Y or Z axis
- 2. Vibration specifications assume that the SSD is mounted securely with the input vibration applied to the drive mounting screws. Stimulus may be applied in the X, Y or Z axis. The measured specification is in root mean squared form.



#### 1.2.14. Electromagnetic Immunity

Electromagnetic Immunity tests assume the SSD is properly installed in the representative host system. The drive operates properly without errors degradation in performance when subjected to radio frequency (RF) environments defined in the following table.

Test	Description	Performance criteria	Reference standard
Electrostatic discharge	Contact ±4KV Air: ±8KV	А	IEC 61000-4-2:2008
Electrostatic discharge	Contact ±6KV Air: ±12KV	В	IEC 61000-4-2:2008
Electrostatic discharge	Contact ±8KV Air: ±15KV	С	IEC 61000-4-2:2008
Radiated RF immunity	80~1000MHz, 3V/m, 80% AM with 1 KHz sine 900 MHz, 3 V/m, 50% pulse modulation at 200Hz	A	IEC 61000-4-3:2008
Electrical fast transient	±1KV on AC mains ±0.5KV on external I/O	В	IEC 61000-4-4:2004 +Corr.1:2006 +Corr.2:2007
Surge immunity	±1KV differential ±2KV common, AC mains	В	IEC 61000-4-5:2005
Conducted RF immunity	150KHz~80 MHz, 3 Vrms, 80% AM with 1KHz sine	A	IEC 61000-4-6:2008
Power frequency magnetic field	50Hz, 1A/m (r.m.s.)	A	IEC 61000-4-6:2008

#### **Table 12 Radio Frequency Specifications**

#### Notes:

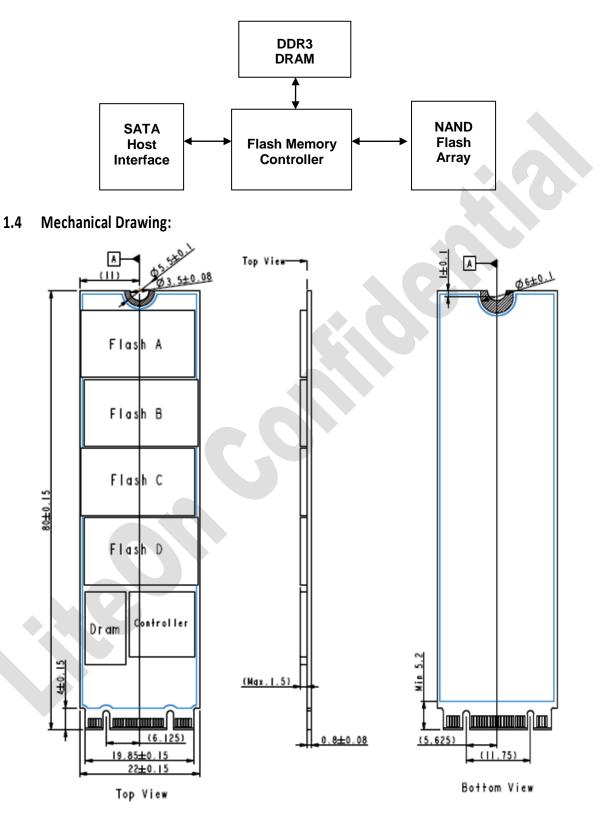
- 1. Performance criterion A = The device shall continue to operate as intended, i.e., normal unit operation with no degradation of performance.
- 2. Performance criterion B = The device shall continue to operate as intended after completion of test, however, during the test, some degradation of performance is allowed as long as there is no data loss operator intervention to restore device function.
- 3. Performance criterion C = Temporary loss of function is allowed. Operator intervention is acceptable to restore device function.
- 4. Contact electrostatic discharge is applied to drive enclosure.

#### 1.2.15. Weight: 10 g Max.

1.2.16. Dimension: 80.0 mm x 22.0 mm x 2.3 mm (L x W x H)



**1.3** Functional Block Diagram



Dimension: 80.0 mm x 22.0 mm x 2.3 mm (L x W x H)



#### 1.5 Architecture

The **CV8-8EXXX 3D TLC series** SATA 6Gb/s Solid State Drive (SSD) utilizes a cost effective system-on-chip (SoC) design to provide a full 6Gb/s bandwidth with the host while managing multiple flash memory devices on multiple channels internally.

#### 1.6 **DEVSLP** power mode

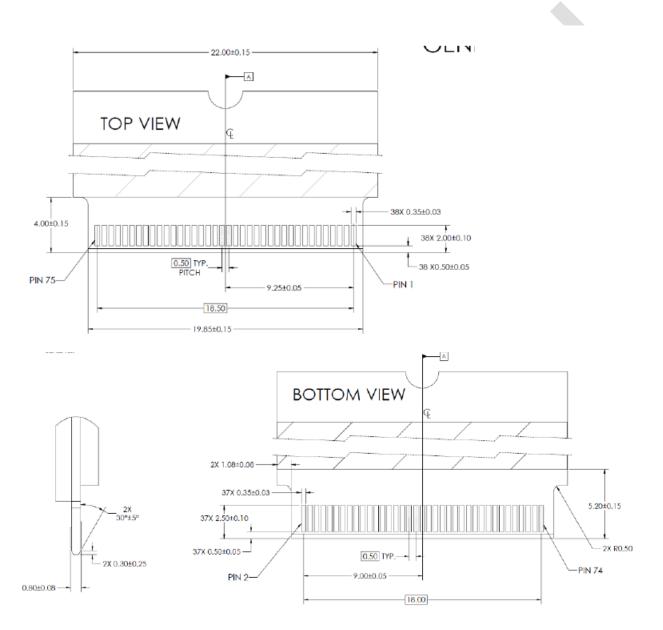
LiteON SSD support DEVSLP power mode. After power up, and enabled by a SET FEATURES command from the host, device will enter DEVSLP mode from any state after receive HW DEVSLP signal pin trigger. And return to Reset state after HW DEVSLP signal pin negated.



### 2 Pin Locations and Signal Descriptions

#### 2.1 Pin Locations

The data and power connector pin locations of the **CV8-8EXXX 3D TLC** series SATA 6 Gb/s SSD are as shown below.





#### 2.2 Signal Descriptions

#### **Table 13 Connector Pin Definitions**

Name	Туре	Description	
P1	CONFIG 3	This pin is follow standard spec connect to ground.	
P1 P2	3.3V AUX		
		Supply pin, 3.3V	
P3	GND	Ground	
P4	3.3V AUX	Supply pin, 3.3V	
P5	Not Available	no connect on SSD	
P6	Not Available	no connect on SSD	
P7	Not Available	no connect on SSD	
P8	Not Available	no connect on SSD	
P9	Not Available	no connect on SSD	
P10	DAS#	Device Activity Signal	
P11	Not Available	no connect on SSD	
P12	(removed for key)	Mechanical Notch B (Removed for Key)	
P13	(removed for key)	Mechanical Notch B(Removed for Key)	
P14	(removed for key)	Mechanical Notch B (Removed for Key)	
P15	(removed for key)	Mechanical Notch B (Removed for Key)	
P16	(removed for key)	Mechanical Notch B (Removed for Key)	
P17	(removed for key)	Mechanical Notch B (Removed for Key)	
P18	(removed for key)	Mechanical Notch B (Removed for Key)	
P19	(removed for key)	Mechanical Notch B (Removed for Key)	
P20	Not Available	no connect on SSD	
P21	CONFIG_0	This pin is follow standard spec connect to ground.	
P22	Not Available	no connect on SSD	
P23	Not Available	no connect on SSD	
P24	Not Available	no connect on SSD	
P25	Not Available	no connect on SSD	
P26	Not Available	no connect on SSD	
P27	GND	Ground	
P28	Not Available	no connect on SSD	
P29	Not Available	no connect on SSD	
P30	Not Available	no connect on SSD	
P31	Not Available	no connect on SSD	
P32	Not Available	no connect on SSD	
P33	GND	Ground	
P34	Not Available	no connect on SSD	
P35	Not Available	no connect on SSD	
P36	Not Available	no connect on SSD	
P37	Not Available	no connect on SSD	
		If system didn't support DEVSLP, set Device Sleep Signal high and	
		keep (from power on), device will ignore.	
		If system support DEVSLP, set Device Sleep Signal low (from	
P38	Device Sleep Signal	power on) device, device will support DEVSLP function as below:	
		Device Sleep Signal H: SSD enter sleep model.	
		Device Sleep Signal L: SSD exit sleep model.	
P39	GND	Ground	
P40	Not Available	no connect on SSD	
P41	SATA-B+/PETn0	Host receiver differential signal pair	
P42	Not Available	no connect on SSD	
P43	SATA-B-/PETp0	Host receiver differential signal pair	
175	3/1/10/11/100		



Name	Туре	Description
P44	Not Available	no connect on SSD
P45	GND	Ground
P46	Not Available	no connect on SSD
P47	SATA-A-/PERn0	Host transmitter differential signal pair
P48	Not Available	no connect on SSD
P49	SATA-A+/PERp0	Host transmitter differential signal pair
P50	Not Available	no connect on SSD
P51	GND	Ground
P52	Not Available	no connect on SSD
P53	Not Available	no connect on SSD
P54	Not Available	no connect on SSD
P55	Not Available	no connect on SSD
P56	MFG1	Manufacturing pin. Use determined by vendor. Must be a no-
P30	WIFGI	connect on the host board
P57	GND	Ground
P58	MFG2	Manufacturing pin. User determined by vendor. Must be a no-
F JO	IVIFGZ	connect on a host board
P59	(removed for key)	Mechanical Notch M (Removed for Key)
P60	(removed for key)	Mechanical Notch M (Removed for Key)
P61	(removed for key)	Mechanical Notch M (Removed for Key)
P62	(removed for key)	Mechanical Notch M (Removed for Key)
P63	(removed for key)	Mechanical Notch M (Removed for Key)
P64	(removed for key)	Mechanical Notch M (Removed for Key)
P65	(removed for key)	Mechanical Notch M (Removed for Key)
P66	(removed for key)	Mechanical Notch M (Removed for Key)
P67	Not Available	no connect on SSD
P68	SUSCLK	no connect on SSD
P69	CONFIG_1	This pin is follow standard spec connect to ground.
P70	3.3V AUX	Supply pin, 3.3V
P71	GND	Ground
P72	3.3V AUX	Supply pin, 3.3V
P73	GND	Ground
P74	3.3V AUX Supply pin	
P75	CONFIG_2	This pin is follow standard spec connect to ground.



### **3 ATA Command Sets**

#### 3.1 ATA Command

The SSD supports all the mandatory ATA commands defined in the ATA/ATAPI-8 specification.

#### 3.1.1 ATA General Feature Command Set

The SSD supports the ATA General feature Command set (non-packet), which consists of

- EXECUTE DEVICE DIAGNOSTIC
- FLUSH CACHE
- IDENTIFY DEVICE
- · READ DMA
- · READ DMA WITHOUT RETRIES
- READ SECTOR(S)
- READ SECTORS(S) WITHOUT RETRIES
- READ VERIFY SECTORS(S)
- READ VERIFY SECTORS(S) WITHOUT RETRIES
- SEEK
- SET FEATURES
- · WRITE DMA
- WRITE DMA WITHOUT RETRIES
- WRITE SECTOR(S)
- WRITE SECTOR(S) WITHOUT RETRY
- READ MULTIPLE
- SET MULTIPLE MODE
- WRITE MULTIPLE
- INITIALIZE DEVICE PARAMETERS
- · DATA SET MANAGEMENT
- The SSD supports all the following optional commands
  - READ BUFFER
  - WRITE BUFFER
  - DOWNLOAD MICROCODE



#### 3.1.2 Identify Device Data

The following table details the sector data returned after issuing an IDENTIFY DEVICE command.

Word         V=Variable X=Both         Default Value         Description           0         F         0040h         General configuration bit-significant information           1         F         37FFh         Obsolete-Number of logical cylinders (16,383)           2         F         C837h         Specific configuration           3         F         0000h         Retired           6         F         0007h         Obsolete-Number of logical sectors per logical track (63)           7-8         F         0000h         Retired           10-19         V         Var.         Serial number (20 ASCII characters)           20-22         F         0000h         Retired / Obsolete           23-26         V         Var.         Firmware revision (8 ASCII characters)           20-42         F         0000h         Retired / Obsolete           23-26         V         Var.         Model number           44         F         4000h         Trusted Computing feature set options, bit14 should be 1           45         F         0000h         Capabilities           50         F         4000h         Capabilities           51-52         F         0007h         Words 88 and 70:64 valid		Table 14 Returned Sector Data			
1F3FFhObsolete-Number of logical cylinders (16,383)2FC837hSpecific configuration3F0010hObsolete-Number of logical heads (16)4-5F0000hRetired6F003FhObsolete-Number of logical sectors per logical track (63)7-8F0000hRetired9F0000hRetired10-19VVar.Serial number (20 ASCII characters)20-22F0000hRetired / Obsolete23-26VVar.Model number27-46VVar.Model number47F8010hTrusted Computing feature set options, bit14 should be 149F2F00hCapabilities50F4000hTrusted Computing feature set options, bit14 should be 149F2F00hCapabilities51-52F0000hObsolete53F0007hWords 88 and 70:64 valid54VVar.Obsolete-Number of logical cylinders (16,383)55VVar.Obsolete-Number of logical sectors per logical track (63)56VVar.Obsolete-Number of logical sectors for 28-bit commands60-61 $V$ 250,0459,680Total number of user addressable logical sectors for 28-bit commands62F0000hNumber of user addressable logical sectors for 28-bit commands64F0003hPIO modes supported65F0078hMinimum multiword DMA tran		V=Variable X=Both		-	
2FC837hSpecific configuration3F0010hObsolete-Number of logical heads (16)4-5F0000hRetired6F003FhObsolete-Number of logical sectors per logical track (63)7-8F0000hRetired9F0000hRetired10-19VVar.Serial number (20 ASCII characters)20-22F0000hRetired / Obsolete23-26VVar.Firmware revision (8 ASCII characters)27-46VVar.Model number7.0Maximum number of sectors transferred per interrupt on multiple commands48F4000hTrusted Computing feature set options, bit14 should be 149F2700hCapabilities50F4000hCapabilities51-52F0007hWords 88 and 70:64 valid54VVar.Obsolete - Number of logical sectors (16,383)55VVar.Obsolete - Number of logical sectors per logical track (63)56VVar.Obsolete - Number of logical sectors for 28-bit (63)57-58VVar.Capacity((V)inders*heads*sectors)59V01xxhTotal number of user addressable logical sectors for 28-bit (25,045,424 (64GB))60-61V125,045,424 (64GB)commands (DWord)50,118,192(25,663,680)Total number of user addressable logical sectors for 28-bit (28,668)62F0000hMoulti-word DMA transfer cycle time per word <td></td> <td></td> <td></td> <td></td>					
3F0010hObsolete-Number of logical heads (16)4-5F0000hRetired6F003FhObsolete-Number of logical sectors per logical track (63)7-8F0000hRetired10-19VVar.Serial number (20 ASCII characters)20-22F0000hRetired / Obsolete23-26VVar.Firmware revision (8 ASCII characters)27-46VVar.Model number47F8010h7:0 - Maximum number of sectors transferred per interrupt on multiple commands48F4000hCapabilities50F4000hCapabilities51-52F0000hObsolete53F0007hWords 88 and 70:64 valid54VVar.Obsolete - Number of logical cylinders (16,383)55VVar.Obsolete - Number of logical sectors per logical track (63)57-58VVar.Capability59V01xxhNumber of sectors transferred per interrupt on multiple commands60-61V25,045,242Total number of user addressable logical sectors for 28-bit commands62F0000hDbsolete63V0007hMulti-word DMA modes supported/selected64F0003hPIO modes supported65F0078hMinimum PIO transfer cycle time with ORD flow control66F0078hMinimum PIO transfer cycle time with ORD flow control68F<		F			
4-5       F       0000h       Retired         6       F       003Fh       Obsolete-Number of logical sectors per logical track (63)         7-8       F       0000h       Reserved for assignment by the Compact Flash Association         9       F       0000h       Retired         10-19       V       Var.       Serial number (20 ASCII characters)         20-22       F       0000h       Retired / Obsolete         23-26       V       Var.       Model number         27-46       V       Var.       Model number         47       F       8010h       Trusted Computing feature set options, bit14 should be 1         48       F       4000h       Capabilities       0         50       F       4000h       Capabilities       0         51-52       F       00007h       Words 88 and 70:64 valid       0         54       V       Var.       Obsolete - Number of logical sectors per logical track (63)         55       V       Var.       Obsolete - Number of logical sectors per logical track (63)         55       V       Var.       Obsolete - Number of logical sectors per logical track (63)         56       V       Var.       Capacity(Cylinders*heads*sectors)					
6F003FhObsolete-Number of logical sectors per logical track (63)7-8F0000hReserved for assignment by the Compact Flash Association9F0000hRetired10-19VVar.Serial number (20 ASCII characters)20-22F0000hRetired / Obsolete23-26VVar.Model number27-46VVar.Model number47F $8010h$ 7:0 - Maximum number of sectors transferred per interrupt on multiple commands48F4000hCapabilities50F4000hCapabilities51-52F0000hObsolete53F0007hWords 88 and 70:64 valid54VVar.Obsolete - Number of logical sectors per logical track (63)55VVar.Obsolete - Number of logical sectors per logical track (63)56VVar.Obsolete - Number of logical sectors per logical track (63)57-58VVar.Capacity(Cylinders*heads*sectors)59V01xxhTotal number of user addressable logical sectors for 28-bit commands60-61(256,680)Total number of DMA modes supported/selected62F0000hObsolete63V0003hPIO modes supported64F0078hMinimum PIO transfer cycle time per word65F0078hMinimum PIO transfer cycle time with 0DMA transfer cycle time66F0078hMinimum PIO transfer cycle tim					
7-8F0000hReserved for assignment by the Compact Flash Association9F0000hRetired10-19VVar.Serial number (20 ASCII characters)20-22F0000hRetired / Obsolete23-26VVar.Firmware revision (8 ASCII characters)27-46VVar.Model number47F8010h7.0 – Maximum number of sectors transferred per interrupt on multiple commands48F4000hTrusted Computing feature set options, bit14 should be 149F2200hCapabilities50F4000hCapabilities51-52F0000hObsolete53F0007hWords 88 and 70:64 valid54VVar.Obsolete - Number of logical cylinders (16,383)55VVar.Obsolete - Number of logical sectors per logical track (63)56VVar.Capacity(Cylinders*heads*sectors)59V01xxhNumber of sectors transferred per interrupt on multiple commands60-61V250,069,680 (1286B)Total number of user addressable logical sectors for 28-bit (2866B)62F0000hObsolete63V003hPIO modes supported/selected64F0078hMinimum multiword DMA transfer cycle time per word66F0078hMinimum PIO transfer cycle time with IORDY flow control68F0078hMinimum PIO transfer cycle time with IORDY flow control		F			
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23-26       V       Var.       Firmware revision (8 ASCII characters)         27-46       V       Var.       Model number         47       F       8010h       7:0 - Maximum number of sectors transferred per interrupt on multiple commands         48       F       4000h       Trusted Computing feature set options, bit14 should be 1         49       F       2F00h       Capabilities         50       F       4000h       Capabilities         51-52       F       0000h       Obsolete         53       F       0007h       Words 88 and 70:64 valid         54       V       Var.       Obsolete - Number of logical cylinders (16,383)         55       V       Var.       Obsolete - Number of logical sectors per logical track (63)         56       V       Var.       Capacity(Cylinders*heads*sectors)         59       V       01xxh       Commands         60-61       V       250,069,680       Total number of user addressable logical sectors for 28-bit (126GB)         62       F       0000h       Obsolete       Obsolete         63       V       0007h       Multi-word DMA modes supported/selected         64       F       0003h       PIO modes supported         65	10-19	V	Var.	Serial number (20 ASCII characters)	
27-46       V       Var.       Model number         47       F       8010h       7:0 - Maximum number of sectors transferred per interrupt on multiple commands         48       F       4000h       Trusted Computing feature set options, bit14 should be 1         49       F       2F00h       Capabilities         50       F       4000h       Capabilities         51-52       F       0000h       Obsolete         53       F       0007h       Words 88 and 70:64 valid         54       V       Var.       Obsolete - Number of logical cylinders (16,383)         55       V       Var.       Obsolete - Number of logical sectors per logical track (63)         56       V       Var.       Obsolete - Number of logical sectors per logical track (63)         57-58       V       Var.       Obsolete - Number of logical sectors per logical track (63)         59       V       01xh       Number of sectors transferred per interrupt on multiple commands         60-61       V       225,045,424 (64GB)       commands (DWord)         500,118,192       (256GB)       00solete       commands (DWord)         62       F       0003h       PIO modes supported/selected       64         64       F       0007h	20-22	F	0000h	Retired / Obsolete	
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51-52       F       0000h       Obsolete         53       F       0007h       Words 88 and 70:64 valid         54       V       Var.       Obsolete - Number of logical cylinders (16,383)         55       V       Var.       Obsolete - Number of logical heads (16)         56       V       Var.       Obsolete - Number of logical sectors per logical track (63)         57-58       V       Var.       Capacity(Cylinders*heads*sectors)         59       V       01xxh       Number of sectors transferred per interrupt on multiple commands         60-61       V       250,069,680       Total number of user addressable logical sectors for 28-bit commands (DWord)         500,118,192       (256GB)       250,069,680       Total number of user addressable logical sectors for 28-bit commands (DWord)         62       F       0000h       Obsolete       0007h         63       V       0007h       Multi-word DMA modes supported/selected         64       F       0003h       PIO modes supported         65       F       0078h       Manufacture's recommended multiword DMA transfer cycle time per word         66       F       0078h       Manufacture's recommand overlap and queuing)         71-74       F       0000h       Reserved(for future comma	49	F	2F00h	Capabilities	
53       F       0007h       Words 88 and 70:64 valid         54       V       Var.       Obsolete - Number of logical cylinders (16,383)         55       V       Var.       Obsolete - Number of logical neads (16)         56       V       Var.       Obsolete - Number of logical sectors per logical track (63)         57-58       V       Var.       Capacity(Cylinders*heads*sectors)         59       V       01xxh       Capacity(Cylinders*heads*sectors)         60-61       V       250,069,680       Total number of user addressable logical sectors for 28-bit commands         60-61       V       250,069,680       Total number of USCA       Capacity(Cylinders*heads*sectors)         60-61       V       250,069,680       Total number of user addressable logical sectors for 28-bit commands (DWord)         500,118,192       (256GB)       Commands       Capacity(Cylinders*heads*sector)         62       F       0000h       Obsolete       Capacity(Cylinders*heads*sector)         63       V       0007h       Multi-word DMA modes supported/selected         64       F       0003h       PIO modes supported         65       F       0078h       Manufacture's recommended multiword DMA transfer cycle time         67       F       0078h <td>50</td> <td>F</td> <td>4000h</td> <td>Capabilities</td>	50	F	4000h	Capabilities	
54       V       Var.       Obsolete - Number of logical cylinders (16,383)         55       V       Var.       Obsolete - Number of logical heads (16)         56       V       Var.       Obsolete - Number of logical sectors per logical track (63)         57-58       V       Var.       Capacity(Cylinders*heads*sectors)         59       V       01xxh       Number of sectors transferred per interrupt on multiple commands         60-61       V       250,069,680       Total number of user addressable logical sectors for 28-bit commands (DWord)         60-61       V       250,069,680       Total number of UW Cylinders sectors for 28-bit commands (DWord)         62       F       0000h       Obsolete         63       V       0007h       Multi-word DMA modes supported/selected         64       F       0003h       PIO modes supported         65       F       0078h       Manufacture's recommended multiword DMA transfer cycle time per word         66       F       0078h       Minimum PIO transfer cycle time with URDY flow control         68       F       0078h       Minimum PIO transfer cycle time with URDY flow control         69-70       F       0000h       Reserved for the IDENTIFY packet DEVICE command         71-74       F       0000h	51-52	F	0000h	Obsolete	
55       V       Var.       Obsolete - Number of logical heads (16)         56       V       Var.       Obsolete - Number of logical sectors per logical track (63)         57-58       V       Var.       Capacity(Cylinders*heads*sectors)         59       V       01xxh       Number of sectors transferred per interrupt on multiple commands         60-61       V       125,045,424 (64GB)       Total number of user addressable logical sectors for 28-bit commands         60-61       V       250,069,680       Total number of user addressable logical sectors for 28-bit commands (DWord)         500,118,192       (256GB)       500,118,192       commands (DWord)         62       F       0000h       Obsolete         63       V       0007h       Multi-word DMA modes supported/selected         64       F       0003h       PIO modes supported         65       F       0078h       Minimum PIO transfer cycle time per word         66       F       0078h       Minimum PIO transfer cycle time with IORDY flow control         68       F       0078h       Minimum PIO transfer cycle time with IORDY flow control         69-70       F       0000h       Reserved (for future command overlap and queuing)         71-74       F       0000h       Reserved for	53	F	0007h	Words 88 and 70:64 valid	
56       V       Var.       Obsolete - Number of logical sectors per logical track (63)         57-58       V       Var.       Capacity(Cylinders*heads*sectors)         59       V       01xxh       Number of sectors transferred per interrupt on multiple commands         60-61       V       125,045,424 (64GB)       Total number of user addressable logical sectors for 28-bit commands         60-61       V       250,069,680 (128GB)       Total number of user addressable logical sectors for 28-bit commands (DWord)         500,118,192 (256GB)       500,118,192 (256GB)       commands (DWord)         62       F       0000h       Obsolete         63       V       0007h       Multi-word DMA modes supported/selected         64       F       0003h       PIO modes supported         65       F       0078h       Minimum multiword DMA transfer cycle time per word         66       F       0078h       Minimum PIO transfer cycle time without flow control         68       F       0078h       Minimum PIO transfer cycle time with IORDY flow control         69-70       F       0000h       Reserved for the IDENTIFY packet DEVICE command         75       F       001Fh       4:0 Maximum Queue depth-1=31         76       V       070Eh       Serial ATA capabilit	54	V	Var.	Obsolete - Number of logical cylinders (16,383)	
57-58       V       Var.       Capacity(Cylinders*heads*sectors)         59       V       01xxh       Number of sectors transferred per interrupt on multiple commands         60-61       125,045,424 (64GB)       Total number of user addressable logical sectors for 28-bit commands (DWord)         60-61       250,069,680 (128GB)       Total number of user addressable logical sectors for 28-bit commands (DWord)         62       F       0000h       Obsolete         63       V       0007h       Multi-word DMA modes supported/selected         64       F       0003h       PIO modes supported         65       F       0078h       Minimum multiword DMA transfer cycle time per word         66       F       0078h       Minimum PIO transfer cycle time without flow control         68       F       0078h       Minimum PIO transfer cycle time with IORDY flow control         69-70       F       0000h       Reserved(for future command overlap and queuing)         71-74       F       0000h       Reserved for the IDENTIFY packet DEVICE command         75       F       001Fh       4:0 Maximum Queue depth-1=31         76       V       070Eh       Serial ATA capabilities         77       V       Var.       Reserved for Serial ATA	55	V	Var.	Obsolete - Number of logical heads (16)	
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59VUIXN commands60-61V125,045,424 (64GB) 250,069,680 (128GB)Total number of user addressable logical sectors for 28-bit commands (DWord)60-61V250,069,680 (128GB)Total number of user addressable logical sectors for 28-bit commands (DWord)62F0000hObsolete63V0007hMulti-word DMA modes supported/selected64F0003hPIO modes supported65F0078hMinimum multiword DMA transfer cycle time per word66F0078hMinimum PIO transfer cycle time without flow control68F0078hMinimum PIO transfer cycle time without flow control69-70F0000hReserved(for future command overlap and queuing)71-74F0000hReserved for the IDENTIFY packet DEVICE command75F001Fh4:0 Maximum Queue depth-1=3176V070EhSerial ATA capabilities77VVar.Reserved for Serial ATA	57-58	V	Var.	Capacity(Cylinders*heads*sectors)	
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66F0078hManufacture's recommended multiword DMA transfer cycle time67F0078hMinimum PIO transfer cycle time without flow control68F0078hMinimum PIO transfer cycle time with IORDY flow control69-70F0000hReserved(for future command overlap and queuing)71-74F0000hReserved for the IDENTIFY packet DEVICE command75F001Fh4:0 Maximum Queue depth-1=3176V070EhSerial ATA capabilities77VVar.Reserved for Serial ATA	64	F	0003h	PIO modes supported	
67F0078hMinimum PIO transfer cycle time without flow control68F0078hMinimum PIO transfer cycle time with IORDY flow control69-70F0000hReserved(for future command overlap and queuing)71-74F0000hReserved for the IDENTIFY packet DEVICE command75F001Fh4:0 Maximum Queue depth-1=3176V070EhSerial ATA capabilities77VVar.Reserved for Serial ATA	65	F	0078h	Minimum multiword DMA transfer cycle time per word	
68F0078hMinimum PIO transfer cycle time with IORDY flow control69-70F0000hReserved(for future command overlap and queuing)71-74F0000hReserved for the IDENTIFY packet DEVICE command75F001Fh4:0 Maximum Queue depth-1=3176V070EhSerial ATA capabilities77VVar.Reserved for Serial ATA	66	F	0078h	Manufacture's recommended multiword DMA transfer cycle time	
69-70F0000hReserved(for future command overlap and queuing)71-74F0000hReserved for the IDENTIFY packet DEVICE command75F001Fh4:0 Maximum Queue depth-1=3176V070EhSerial ATA capabilities77VVar.Reserved for Serial ATA	67	F	0078h	Minimum PIO transfer cycle time without flow control	
71-74F0000hReserved for the IDENTIFY packet DEVICE command75F001Fh4:0 Maximum Queue depth-1=3176V070EhSerial ATA capabilities77VVar.Reserved for Serial ATA	68	F	0078h	Minimum PIO transfer cycle time with IORDY flow control	
75F001Fh4:0 Maximum Queue depth-1=3176V070EhSerial ATA capabilities77VVar.Reserved for Serial ATA	69-70	F	0000h	Reserved(for future command overlap and queuing)	
75F001Fh4:0 Maximum Queue depth-1=3176V070EhSerial ATA capabilities77VVar.Reserved for Serial ATA	71-74	F	0000h	Reserved for the IDENTIFY packet DEVICE command	
76V070EhSerial ATA capabilities77VVar.Reserved for Serial ATA	75	F	001Fh	4:0 Maximum Queue depth-1=31	
77 V Var. Reserved for Serial ATA	76	V			
	77	V			
		V			

#### Table 14 Returned Sector Data



Word	F=Fixed V=Variable X=Both	Default Value	Description	
79	V	Var.	Serial ATA features enabled	
80	F	01FEh	Major Version Number	
81	F	0021h	Minor Version Number	
82	F	346Bh	Commands and feature sets supported	
83	F	7D01h	Commands and feature sets supported	
84	F	4123h	Commands and feature sets supported	
85	V	3469h	Commands and feature sets supported or enabled	
86	V	BC01h	Commands and feature sets supported or enabled	
87	F	4023h	Commands and feature sets supported or enabled	
88	V	407Fh	Ultra DMA modes	
89	F	0003h	Time required for security erase unit completion	
90	F	0003h	Time required for enhanced security erase completion	
91	F	0000h	Current advanced power management value	
92	V	Var.	Master Password Identifier	
			Hardware reset result. The contents of bits (12:0) of this word	
93	V	0000h	shall change only during the execution of a hardware reset.	
94	F	0000h	Current AAM value	
95	F	0000h	Stream Minimum Request Size	
96	F	0000h	Streaming Transfer Time - DMA	
97	F	0000h	Streaming Access Latency - DMA and PIO	
98-99	F	0000h	Streaming Performance Granularity	
50 55		125,045,424		
		(64GB)		
100-103	V	250,069,680 (128GB)	Maximum user LBA for 48-bit Address feature set	
		500,118,192		
		(256GB)		
104	F	0000h	Streaming Transfer Time - PIO	
105	F	0008h	Maximum number of 512-byte blocks per DATA SET MANAGEMENT command	
106	F	4000h	Physical sector size/logical sector size	
100	F	0000h	Inter-seek delay for ISO-7779 acoustic testing in microseconds	
108-111	V	0000h 0000h 0000h 0000h	World wide name	
112-115	F	0000h	Reserved for word wide name extension to 128 bits	
116	F	0000h	Reserved for TLC	
117-118	F	0000h	Words per logical sector	
119	F	4010h	Commands and feature sets supported	
120	F	4010h	Commands and feature sets supported or enabled	
121-126	F	0000h	Reserved for expanded supported and enabled settings	
127	F	0000h	Removable Media Status Notification feature set support	
128	V	002xh	Security status	
129-159	F	0000h	Vendor specific	
160	F	0000h	Compact Flash Association (CFA) power mode 1	
161-167	F	0000h	Reserved for the CompactFlash Association	
161-167	F	0000h		
168	F	0000h	DATA SET MANAGEMENT command is supported	
170-173	г V	Var.	Additional Product Identifier (ATA String)	
170-173	F	0000h		
1/4-1/3	Г	000011	Reserved	

## LT EON

Word	F=Fixed V=Variable X=Both	Default Value	Description
176-205	F	0000h	Current media serial number (ATA string)
206	F	003Dh	SCT Command Transport
207-208	F	0000h	Reserved
209	F	4000h	Alignment of logical blocks within a physical block
210-211	F	0000h	Write-Read-Verify Sector Count Mode 3 (DWord)
212-213	F	0000h	Write-Read-Verify Sector Count Mode 2 (DWord)
214	F	0000h	NV Cache Capabilities
215-216	F	0000h	NV Cache Size in Logical Blocks (DWord)
217	F	0001h	Nominal media rotation rate
218	F	0000h	Reserved
219	F	0000h	NV Cache Options
220	F	0000h	7:0 Write-Read-Verify feature set current mode
221	F	0000h	Reserved
222	F	1075h	Transport major version number
223	F	0000h	Transport minor version number
224-229	F	0000h	Reserved
230-233	F	0000h	Extended Number of User Addressable Sectors (QWord)
234	F	0000h	Minimum number of 512-byte data blocks per DOWNLOAD MICROCODE command for mode 03h
235	F	0000h	Minimum number of 512-byte data blocks per DOWNLOAD MICROCODE command for mode 03h
236-254	F	0000h	Reserved
255	V	Var.	Integrity word

Note:

1. F=Fixed. The content of the word is fixed and does not change for removable media devices, these values may change when media is Removed or changed.

- 2. V=Variable. The state of at least one bit in a word is variable and may change depending on the state of the device or the commands executed by the device.
- 3. X=F or V. The content of the word may be fixed or variable.

#### 3.2 Power Management Command Set

The SSD supports the power management command set, which consists of

CHECK POWER MODE

- IDLE
- IDLE IMMEDIATE
- SLEEP
- STANDBY
- · STANDBY IMMEDIATE



#### 3.3 Security Mode Feature Set

The SSD supports the Security Mode command set, which consist of

- · SECURITY SET PASSWORD
- SECURITY UNLOCK
- SECURITY ERASE PREPARE
- SECURITY ERASE UNIT
- · SECURITY FREEZE LOCK
- SECURITY DISABLE PASSWORD

#### 3.4 SMART Command Set

The SSD supports the SMART command set, which consist of

- SMART ENABLE OPERATIONS
- SMART DISABLE OPERATIONS
- · SMART ENABLE/DISABLE AUTOSAVE
- SMART RETURN STATUS

The SSD supports the following optional commands.

- SMART EXECUTE OFF-LINE IMMEDIATE
- SMART READ DATA
- SMART READ LOG
- SMART WRITE LOG

The table below lists the SMART commands.

#### Table 15 SMART commands

Subcommand	Code	LBA Low value
SMART ATTRIBUTE VALUES (READ DATA)	D0h	
READ ATTRIBUTE THRESHOLDS	D1h	
ENABLE/DISABLE ATTRIBUTE AUTOSAVE	D2h	
SAVE ATTRIBUTE VALUES	D3h	
EXECUTE OFF-LINE IMMEDIATE	D4h	
EXECUTE SMART OFF-LINE ROUTINE		00h
EXECUTE SMART SHORT SELF-TEST ROUTINE (OFFLINE)		01h
EXECUTE SMART EXTENDED SELF-TEST ROUTINE (OFFLINE)		02h
ABORT OFF-LINE ROUTINE		7Fh
EXECUTE SMART SHORT SELF-TEST ROUTINE (CAPTIVE)		81h
EXECUTE SMART EXTENDED SELF-TEST ROUTINE ( CAPTIVE )		82h
READ LOG SECTOR	D5h	
WRITE LOG SECTOR		
ENABLE SMART OPERATIONS		
DISABLE SMART OPERATIONS		
RETURN SMART STATUS		
Enable/Disable Automatic OFFLINE	DBh	

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#### 3.5 Host Protected Area Command Set

The SSD supports the Host Protected Area command set which consists of

- READ NATIVE MAX ADDRESS
- · SET MAX ADDRESS
- READ NATIVE MAX ADDRESS EXT
- · SET MAX ADDRESS EXT

The SSD supports the following optional commands.

- · SET MAX SET PASSWORD
- · SET MAX LOCK
- · SET MAX FREEZE LOCK
- · SET MAX UNLOCK

#### 3.6 48-Bit Address Command Set

The SSD supports the Host Protected Area command set, which consists of

- FLUSH CACHE EXT
- $\cdot$  READ DMA EXT
- · READ NATIVE MAX ADDRESS EXT
- READ SECTOR(S) EXT
- READ VERIFY SECTOR(S) EXT
- READ MULTIPLE EXT
- · SET MAX ADDRESS EXT
- $\cdot$  WRITE DMA EXT
- · WRITE MULTIPLE EXT
- WRITE MULTIPLE FUA EXT
- · WRITE SECTOR(S) EXT

#### 3.7 Device Configuration Overlay Command Set

The SSD supports the Device configuration Overlay command set, which consists of

- DEVICE CONFIGURATION FREEZE LOCK
- DEVICE CONFIGURATION IDENTITY
- DEVICE CONFIGURATION RESTORE
- DEVICE CONFIGURATION SET

#### 3.8 General Purpose log Command Set

The SSD supports the general purpose log command set, which consists of

- READ LOG EXT
- WRITE LOG EXT



### **4 SATA Command Sets**

#### 4.1 SATA Command

The SATA 3.0 Specification is a super set of the ATA/ATAPI-8 specification with regard to supported commands. The SSD supports the following features which are unique to the SATA 3.0 Specification.

#### 4.1.1. Software Settings Preservation

The SSD supports the SET FEATURES parameter to enable/disable the preservation of software settings.

#### 4.1.2. Native Command Queuing

The SSD supports the Native Command Queuing (NCQ) command set, which includes.

- · READ FPDMA QUEUED
- WRITE FPDMA QUEUED

Note: with a maximum queue depth equal to 32



## **5** References

This document references standards defined by a variety of organizations as listed below.

Date	Title	Location
Dec 2008	VCCI	http://www.vcci.or.jp/vcci_e/general/jo in/index.html
July 2007	ROHS	Search for material description datasheet at http://intel.pcnalert.com
July 2007	SFF-8144, 1.8" drive form factor	http://www.sffcommittee.org
February 2007	Serial ATA Revision 2.6	http://www.sata-io.org
May 2006	SFF-8223, 2.5" Drive w/Serial Attachment Connector	http://www.sffcommittee.org
May 2005	SFF-8201, 2.5" drive form factor	http://www.sffcommittee.org
April 2004	ATA-7 Spec. Volume 1	http://www.t13.org/
Aug. 2009	ATA-8 Spec. Rev 2	http://www.t13.org/
	International Electro Technical Commission EB61000	
2008	4-2 Personnel Electrostatic Discharge Immunity	
2008	4-3 Electromagnetic compatibility (EMC)	http://www.iec.ch
2004	4-4 Electromagnetic compatibility (EMC)	
2005	4-5 Electromagnetic compatibility (EMC)	
2008	4-6Electromagnetic compatibility (EMC)	
2008	4-11 (Voltage variations)	
2004	ENV 50204 (Radiated electromagnetic field from digital radio telephones)	http://www.iec.ch

#### **Table 16 Standards References**



## 6 Terms and Acronyms

This document incorporates many industry- and device-specific words use the following list to define a variety of terms and acronyms.

	Table 17 Glossary of Terms and Acronyms			
Term	Definition			
ATA	Advanced Technology Attachment			
ΑΤΑΡΙ	Advanced Technology Attachment Packet Interface			
BER	Bit Error Rate, or percentage of bits that have errors relative to the total number of bits received			
BIOS	Basic Input/Output System			
Chipset	A term used to define a collection of integrated components required to make a PC function			
DIPM	Device Initiated Power Management			
DIFIVI	The ability of the device to request SATA link power state changes			
DMA	Direct Memory Access			
DRAM	Dynamic Random Access Memory			
EXT	Extended			
FP	First Party			
GB	Giga-byte defined as 1X10 <sup>9</sup> bytes			
HCI	Host Controller Interface			
нст	Hardware Compatibility Test			
HDD	Hard Disk Drive			
	Host Initiated Power Management			
HIPM	The ability of the host to request SATA link power state changes			
Hot Plug	A term used to describe the removal or insertion of a SATA hard drive when the system is powered on			
IOPS	Input output operations per second			
LBA	Logical Block Address			
LPM	Link Power Management: the ability of the SATA link layer to enter one o two lower power consuming states, partial and slumber			
MB	Mega-bytes defined as 1x10 <sup>6</sup> bytes			
mSATA	Mini-SATA			
MTBF	Mean time between failure			
NCQ	Native Command Queuing			



	The ability of the SATA hard drive to re-order commands in order to maximize the efficiency of gathering data from the platters	
NOP	No operation	
NTFS	NT file system	
OEM	Original Equipment Manufacturer	
OS	Operation System	
Port	The point at which a SATA drive physically connected to the SATA	
RAID	AID Redundant Array of Independent Disks	
RMS	Root Mean Squared	
RPM	Revolutions per Minute	
RTM	Release to Manufacture	
SATA	Serial ATA	
SFF	Small Form Factor	
	Self-Monitoring, Analysis and reporting Technology	
SMART	An open standard for developing hard drive and software systems that automatically monitors a hard drive's health and reports potential problems	
SSD	Solid State Drive	
TBD	To Be Determined	
WHQL	QL Microsoft* Windows Hardware Quality Labs	
Write Cache	A memory device within a hard drive, which is allocated for the temporary storage of data before that data is copied to its permanent storage location	
/CCI Voluntary Control Council for Interface		





## 7 Endurance

Capacity	TBW (Total Bytes Written)
128GB	Up to 146 TB
256GB	Up to 255 TB
512GB	Up to 480 TB

Note: TBW value is derived from JEDEC based on population of SSDs statistics.